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ARTICLE

ENERGY EFFICIENT RELIABLE (2^NX1) MULTIPLEXER DESIGN USING QCA APPROACH

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ABSTRACT

In the fast growing VLSI technology, designing allows power utilizing tool turns into a testing task and leads to the era of Quantum-dot cellular automata (QCA). It is one of the unconventional computing stages with cutting edge technology that has the potential of achieving higher speeds, smaller size, and mainly low power consumption in comparison with CMOS technology. This paper presents an evolutionary approach to investigate and realize a modular 2^N to 1 mux. The design is done using AND & OR blocks. The proposed multiplexer is designed and simulated using the QCA Designer tool 2.0.3 in Windows XP operating system. It is observed that the designed multiplexer is efficient in terms of complexity, area, delay and cell count when compared to the previous designs.

KEY WORDS
4×1 Multiplexer, QCA Designer, Majority Gate, Inverter, Power Dissipation

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INTRODUCTION

QCA Designer is one of the good simulation tools to make exact simulation and design for quantum-dot cell automata (QCA). Complex QCA circuits can be produced utilizing QCA Designer on most standard stages. In Boolean capacity and circuit outlines multiplexer is the primary part and plays a critical part. An intuitive approach is carried out to realize a modular 2^n to 1 mux using AND & OR blocks. A basic MUX uses the basic building blocks such as AND & OR. The main objective is to design an efficient mux which has improved values in terms of cell count, complexity, area, and delay [1-6].

The data is communicated through every cell and not held. Every cell eradicates its own particular state after each cycle of the clock QCA Memory Cell. For designing in QCA, a developer must be able to combine basic utilities and then design it in the QCA Designer tool. To accomplish this simulation engines are integrated into QCA Designer. Basically there are three simulation engines in QCA Designer. The first is a digital logic simulator, which views cells as either invalid or plenarily polarized. The next is a stable state of cells within an outline which is determined by the non-linear approximation engine. The third is a quantum mechanical model of a system which depends on the estimation of two states Hamiltonian [7-9].

Due to large number of cells, experimental data cannot be provided for QCA systems which lead to a problem of implementing precise simulation. However, there are countless small QCA systems which have been developed resulting which a motivation is driven for research and implementation of various circuit designs. This research and implementation can further be used to design a specific or particular system.
The QCA cell is square formed and it comprises of four quantum dots as shown in Figure 1. The electrons possess the contrary corners in the fault free QCA cell due to columbic repulsion and gives two stable configurations logic'0' and logic'1' with polarization P = -1 and P = +1 respectively. There will be no actual discharge in capacitor as in conventional CMOS while changing state from logic'0' to logic'1' in QCA cell. There are four clock signals in the QCA designer tool. These clocks help in preventing any traffic inflow of information [10-12].

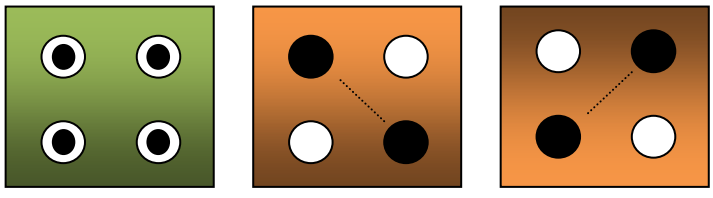

Fig. 1: QCA cell

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As seen from [Fig. 1], four quantum dots are present in a single QCA cell which is organized in a square pattern. 2 extra electrons, which always reside diagonally to each other inside a cell, by tunneling which externally, mutual electrostatic repulsive force is created between these electrons and we can get either of the two logics: logic '0' or logic '1' [13-14]. The synchronize of clock phases is done by using four different clock phases as shown in [Fig. 2].

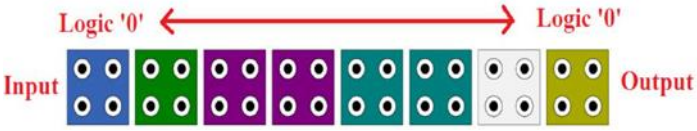


Fig. 2: Clock coding

DESIGN OF NAND & NOR GATE USING QCA

NAND gate design

NAND is one of the two universal gates. NAND is built using AND gate as shown in [Fig. 3]. By inverting the AND output, that is by arranging a cell diagonally to the AND output and keeping it as output we get the NAND gate output.

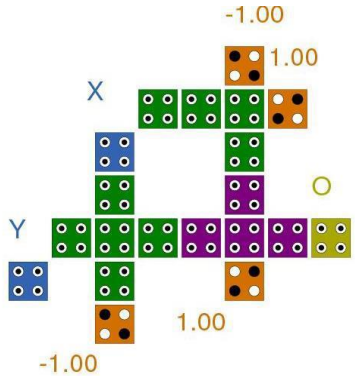


Fig. 3: Design of QCA NAND Gate in QCA Designer

NOR GATE design

NOR is one of the two universal gates. NOR is built using OR gate as shown in [Fig. 4]. By inverting the OR output, that is by arranging a cell diagonally to the OR output and keeping it as output we get the NOR gate output.

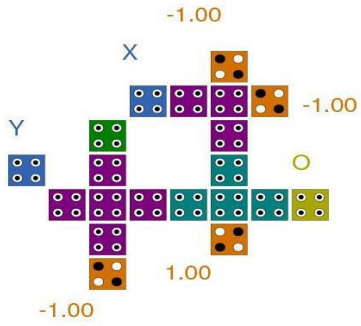


Fig. 4: Design of QCA NOR Gate in QCA Designer

QCA CLOCKING SYSTEM

There are four clock signals in the QCA Designer tool. These clocks help in preventing any traffic inflow of information. Each clock signal will be shifted by a phase of 90. This empowers the information to be pumped through the circuit in view of the dynamic locking and unlatching in cells related to different clock cycles. Using four distinct clock phases synchronization of clock phases in QCA cells is done as shown in [Fig.5].

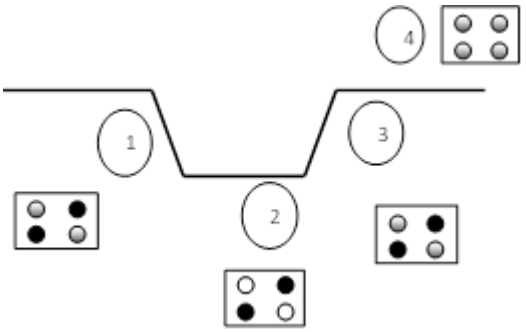
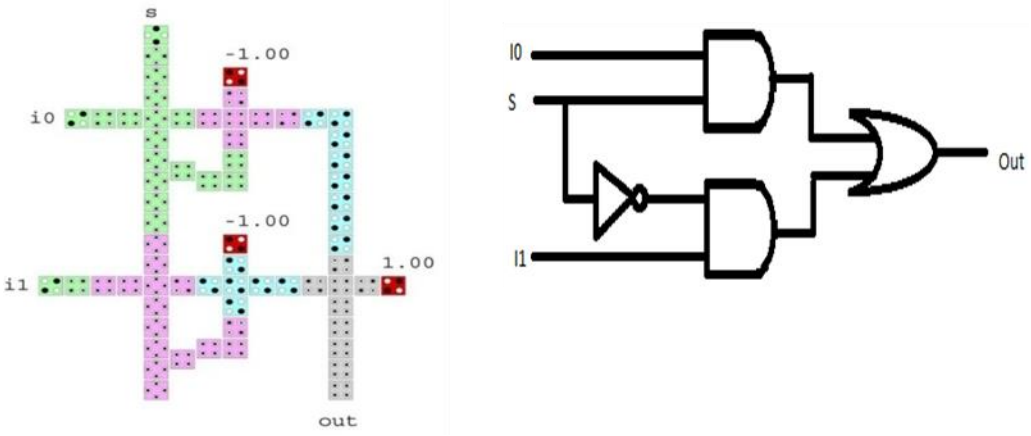


Fig. 5: Stages of the QCA clock

PROPOSED ARCHITECTURE OF MULTIPLEXERS

It can be observed from [Fig. 6] that a 2:1 mux needs three majority gates and one inverter. It can be seen that the inputs 'i0', 'i1' and 's' are put in one clock zone and the outputs are set in another clock zone. The input's' is the select line. This will make the clocking phases to pass over. [Fig. 7] shows the design of 2×1 multiplexer using QCA Designer tool.



(a) (b)

Fig. 6: (a) Existing model of 2×1 Multiplexer (MUX) (b) Symbolic representation of 2×1 multiplexer

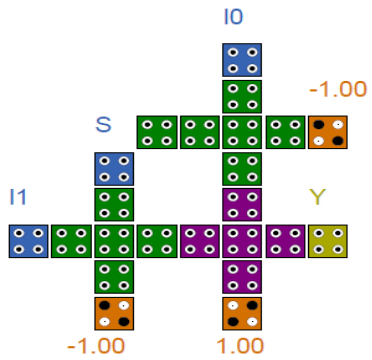


Fig. 7: 2×1 Multiplexer (MUX) design in QCA Designer

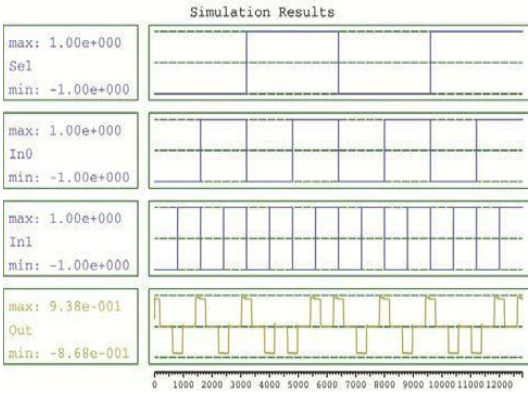


Fig. 8: Simulation results of 2×1 Multiplexer (MUX)

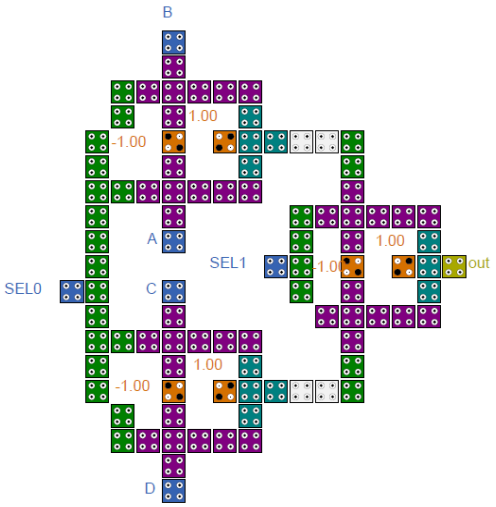


Fig. 9: 4×1 Multiplexer (MUX) design in QCA Designer

[Fig. 8] shows the simulation results of 2×1 MUX. [Fig. 9] shows the design of a 4×1 mux using QCA designer tool. It is observed from the figure that it has four data lines (i0, i1, i2, i3) and two select lines (S0 and S1) of the 4:1 mux. The proposed design uses the concept of the module used for 2:1 mux. [Fig. 10] shows the simulation results of 4×1 multiplexer [15-18].

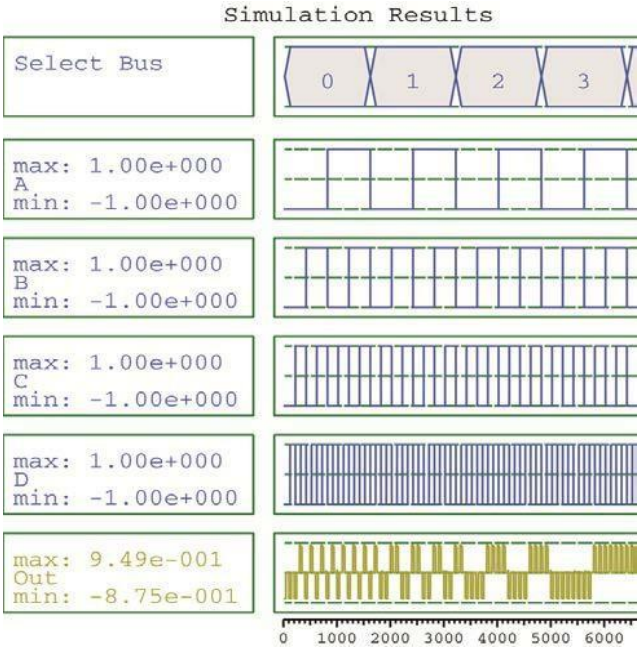


Fig. 10: Simulation results of 4×1 Multiplexer (MUX)

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CONCLUSION

This paper presents an evolutionary approach to explore and realize a modular 2^N to 1 mux. The design is prepared using the AND & OR blocks. The proposed multiplexer is designed and simulated using the QCA Designer tool 2.0.3 in Windows XP operating system. It was observed that the designed multiplexer is efficient in terms of complexity, area, delay and cell count when compared to the previous designs.

CONFLICT OF INTEREST

The authors do not have any conflict of interest.

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FINANCIAL DISCLOSURE

None

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