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DBIST: DYNAMIC BUILT-IN SELF-TEST, DESIGN AND ANALYSIS

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ABSTRACT

Built in self-test (BIST) is widely used in multiprocessor chips due to its high speed property compared to external testing. In addition, it is known that dynamic logic could award high speed to digital systems. However, high energy consumption has been always a limitation in this logic style. In this paper therefore, we are going to propose a dynamic BIST for network on chips and address its clocking energy dissipation. An analytical model is used in order to find the critical paths in the system. Then based on the analytical analysis, a low energy high speed dynamic boundary scan cell is proposed and simulated using HSPICE and a Matlab special purpose simulator. Results reveal significant improvements in terms of performance and energy consumption.

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KEY WORDS

On chip network, testing, modelling, IEEE 1149, low energy, test time, dynamic design

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INTRODUCTION

Testing complex systems such as on-chip networks containing several nodes is a challenging task in terms of energy consumption and test time. Boundary scan test methodology was initially introduced to facilitate the testing of complex PC boards. The IEEE 1149.1 Boundary Scan Test Standard known as JTAG has been widely accepted in the test community [1]. The standard, nevertheless, provides excellent testing features with less complexity for testing of core logic and the interconnections between them. There has been several attempts to apply this approach for multicore systems [2-6]. However, there is still room for more research in this area to carefully examine and optimize its energy and performance. There are several related works in the literature, which the most important reports are briefly reviewed here. In [7], two methodologies are presented to test interconnections network and their test time are evaluated analytically. They proposed aunicast and a multicast testing approaches for 4x4 Mesh and 4-level BFT. They used a model which covers FIFO buffers and switching blocks delay. Three scan chain architectures for core-based ICs, which aim at a minimum test vector set size are presented in [8]. They analyzed their approaches analytically based on the number of pins available to accommodate scan test, as well as the number of scan test patterns and scannable flip flops of each core. In[9], a novel methodology for testing interconnection network architectures is presented and then, foreach switch, the test time is calculated, which is considered to be the sum of the transport latency and the effectivetest time of the switch. Regular and irregular mesh topologies have been taken into account in the test time modelling. The authors of [10] proposed a BIST-based boundary scan architecture to at-speedtest of cross talk faultsfor inter-switch communication links in network on chip.At the end of the paper the number of clocks is calculated using a mathematical simple model same as the approach used in [11].Chakrabarty in [12] presented two lower bound formulations for system on chip testing time models when dedicated bus-based TAM is used. Later in [13] the model was improved and longer test time was resulted compared to the previous versions. Recently, the effect of network topology has been studied on energy and test time of the network on chips using external tester and built in self-test [14]. For that purpose four analytical models were proposed and the chip was simulated analytically. These models were extension of the approaches presented previously in [15, 16]. The same authors presented an approach to reduce test time using a new test algorithm called horizontal vertical test algorithm [17].

As can be seen there are approaches to reduce the energy and delay of the testing in architectural level. However, there is still no attempt to improve the properties of testing in circuit level. Therefore, in this paper, we apply an analytical model to identify the critical path in testing and then using a circuit level approach the critical path will be improved. Our approach could be used together with any other mentioned methods in order to enhance built-in self-testing.

MATERIALS AND METHODS

BIST architecture for multi-core chips

The architecture is shown in **Figure-1** , TPG is test pattern generator and is used to generate test patterns internally in parallel with the other nodes. This block diagram is repeated in other nodes. Test data out (TDO) in each node is connected to test data in (TDI) of the next node to build a serial connection among data registers (DR) of all nodes. In the rest of this paper all the data registers and their connections is called DR. This DR consists the boundary scan cells. Test result register (TRR) is a new architecture to collect the test results and will be explained later in detail. It is located between the DR TDO of the last node and is connected serially. It collects the data in parallel and sends out the results in serial fashion. The EX/INT signal can switch between TPG and TDI. During the test, TPG is activated by enabling INT signal and the test patterns are generated internally. However, initially, the test is governed and started by external controller using TDI. In this case, TPG is deactivated and EX signal enabled.

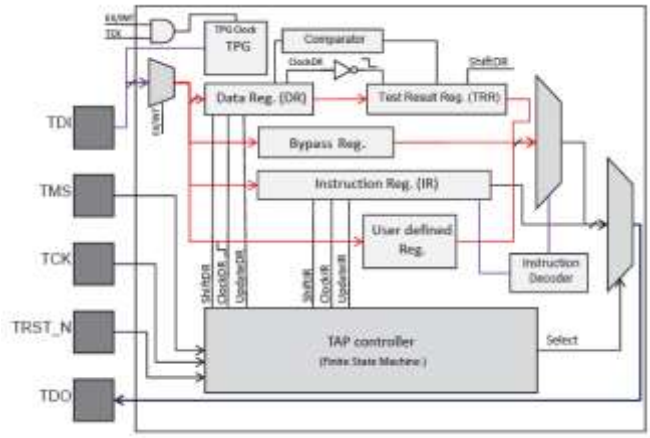

Fig: 1. JTAG architecture used for modeling in this paper

ANALYTICAL MODEL TO ANALYZE THE BIST

In order to examine and optimize the BIST approach in NoCs, we need to calculate both energy and test time in critical paths of the BIST. There are several models proposed in the literature [10, 11, 14-16,18]. Among those, the most suitable models are [16] and [14] for energy and a test time in our application. For completeness, a summary those approaches is given in continue.

Energy Consumption

According to test procedure, testing energy could be divided and written as [16]

$$E_{BIST} = E_{TAP} + E_{IR} + E_{TPG} + E_{DR} + E_{Link} + E_{TRR} \quad (1)$$

, where E_{IR} and E_{TAP} are the energy of instruction register and TAP controller, E_{TPG} is the test pattern generator energy, E_{DR} is the data register energy and E_{Link} is the link energy. The instruction register energy is expressed as

$$E_{IR} = 2n^2 L_{IR}^2 E_{IR_{CELL}} \quad (2)$$

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where *n* is the dimension of *n*×*n* mesh NoC, E_{IRCELL} shown in **Figure-2**, is the energy of a single cell of IR, and L_{IR} is the length of IR in cell.

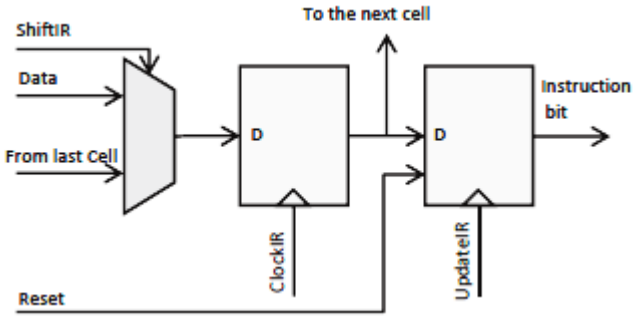

Fig: 2. Instruction register (IR) cell standard implementation [14]

As shown in **Figure- 3**, data register energy is the energy dissipated at input and output boundary scan cells (BSCs) **[igure 3(a) and 3(b) respectively**). Its energy during a complete test procedure is written as

$$E_{DR} = (L_{DR_{avg}} E_{DRshift} + n_{in} E_{DRupdate} + n_{out} E_{DRcapture}) n^2 n_{tp} \quad (3)$$

where, ***E*** *DR shift* is the energy of shifting test data into a BSC, ***E*** *DR update* is the energy of sending test data from BSC to a link, and ***E*** *DR capture* is the energy of loading data from link to a BSC.

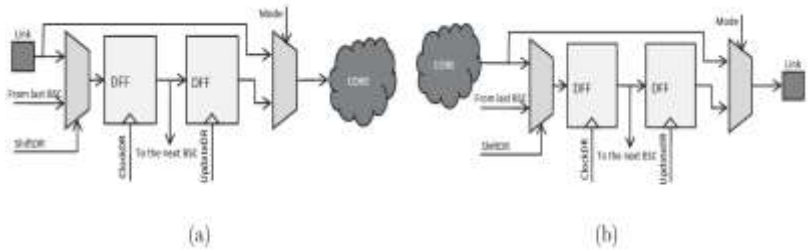

Fig: 3. Input (a) and output (b) boundary scan cells schematic according to IEEE 1149.1 implementation [14].

In addition, $\boldsymbol{L}_{DRavg}$ shown in **Figure-4,** is the average length of DR in unit cell and the Shift, update, and capture energies can be written as

$$E_{DR_i} = E_{MUX}(2) + E_{DFF} \quad (4)$$

, where *i*=DR $_{shift}$, DR $_{capture}$, and DR $_{update}$.
In addition, applying standard IEEE standard TAP [1], a TAP controller could be implemented using 80 two-input NAND gates and 8 DFFs. As a result, the total energy of TAP controller is written as

$$E_{TAP} = n_{tp} n^2 (n_{states} E_{DFF} + n_{NAND} E_{NAND}) \quad (5)$$

wheren_{states} is the number of transitions in DFF during testing of each test pattern, and n_{NAND} is the number of NAND gates used in each TP. Finally, the link energy being the total energy dissipated at input and output links between cores is expressed as

$$E_{Link} = f \alpha_{link} V^2 C_{link} L_{DRavg} n^2 n_{tp} \quad (6)$$

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where V is the supply voltage and C_{link} is the corresponding link energy.

Test time (test delay)

According to [14], the total number of clocks is given as

$$T_{BIST} = \left(12 + 8n^2 L_{IR} + 4n_{tp} L_{DRavg}\right) T_{clk} \quad (7)$$

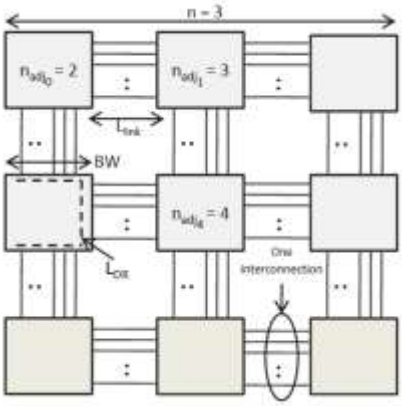

Fig: 4. Number of adjacent nodes and link bandwidth (BW) in NoC with size *n* x *n*, link length *L link*, and mesh structure

The proposed approach to store and shift the results

Comparator

Comparator circuit shown in **Figure-5 ,** is connected to the data register as illustrated in **Figure-6**. Input containing test pattern and output containing test responses are compared using XOR gates. It is worth to mention that in this project only stuck at fault for links are studied. Therefore, input links are compared with output associated links in the neighbor node. Any difference shows a failure in the link. In terms of energy, whenever the data register is updated, comparator consumes energy. As DR is updated by DR shift and DR capture signals thus the comparator energy is written as

$$E_{CMP} = n_{tp} n^2 (E_{CMPshift} + E_{CMPcapture}) \quad (8)$$

where, according to **Figure-5**

$$E_{CMPshift} = L_{DRavg}(L_{DRavg} E_{xor} + E_{or}) \quad (9)$$

and

$$E_{CMPcapture} = n_{int}(E_{xor} + E_{or}) \quad (10)$$

Test Result Register Energy (E_{TRR})

An especial register is devised here to store the result of testing of the links. Shift DR and Capture DR signals are used at MUX's selectors to control shifting and storing data. Two actions are defined on test result register, being storing test results and shifting them out. Each cell of TRR illustrated in **Figure-6**, works as follows. If the data register is updated when the test data are shifted into the DR, then Update DR=1 and the TRRs are reset. In the next step, when Shift DR=0 and Capture DR=1 showing that the test data is captured at the other end of the link. Thus the comparator compares the data at the rising edge and the TRR cell stores the result into the TRRs at the falling edge using the input MUX. It is worth to mention that the inverter on the Clock DR signal separates the actions on rising and falling edges of

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the Clock DR. The next action is shifting test results out the NoC. This happens when Shift DR=1 during EXTEST and PRELOAD instructions. The DFFs are serially connected to each other and form a shift register, which is connected to the TDO signal. This shift register is shown in **Figure-6** at the upper right corner. The length of this shift register is equal to the n_{int}. Energy of TRR shown in **Figure-6,** is given as

$$E_{TRR} = E_{TRRShift} + E_{TRRUpdate} \quad (11)$$

where$E_{TRR\ shift}$ is the energy of TRR due to shifting n_{tp} test patterns given as

$$E_{TRRShift} = n_{tp}\, n_{int}^2\, (E_{DFF} + E_{MUX} + E_{inv}) \quad (12)$$

considering that for each interconnection there is only one DFF to store the test result. In addition, the updating energy for n_{tp} times is written as

$$E_{TRRUpdate} = n_{tp}\, n_{int}\, (E_{DFF} + E_{MUX} + E_{inv}) \quad (13)$$

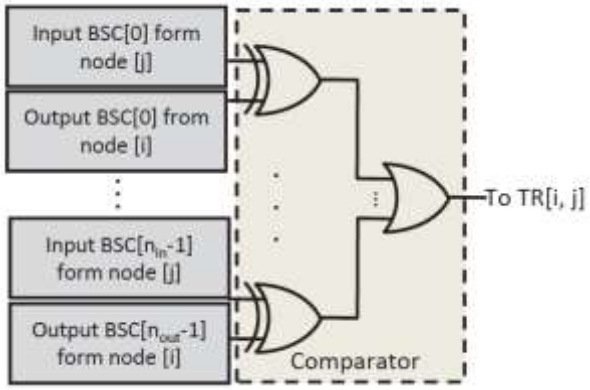


Fig:5. Comparator circuit used in the proposed test architecture

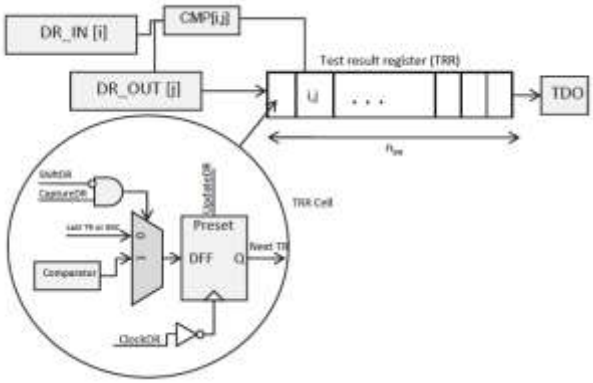


Fig: 6.The proposed mechanism to store and shift out test results is based on the test result register cell shown in this Figure

Dynamic BIST

Critical path analysis

Based on the definition of clock period (T_{clk}) being the maximum time which is required to finish each state of the TAP controller, it is written as

$$T_{clk} = \max(T_{IR-Capture} + T_{IR-Update} + T_{DR-Capture} + T_{DR-Update,\dots}) \quad (14)$$

In addition, based the structure of the input and output BSCs shown in **Figure-5(a)** and **5(b)** respectively, the maximum delay is attributed to DR-Update. We verified our opinion using HSPICE simulation of the BSC and a typical link. Therefore, T_{clk} is equal to the delay of the DR-Update which is given as

$$T_{UpdateDR} = T_{FF} + 2T_{MUX(2)} + T_{Link} \quad (15)$$

where propagation delay T_i is written as

$$T_i = Ln(2)R_{on}C_{on} \quad (16)$$

In which *i* could be FF, two-input multiplexer, Link, and R_{on} and C_{out} are the on-state gate critical path resistance and output capacitance of the circuit respectively. Based on above argument, any possible improvement should be in this architecture. Furthermore, simulation results carried out using the analytical model shown in **Figure-7**, indicate that the BSC or DR is also the bottle neck of the system in terms of energy consumption. Therefore, any approach with high energy consumption overhead will affect the total energy dissipation significantly which is not desired.

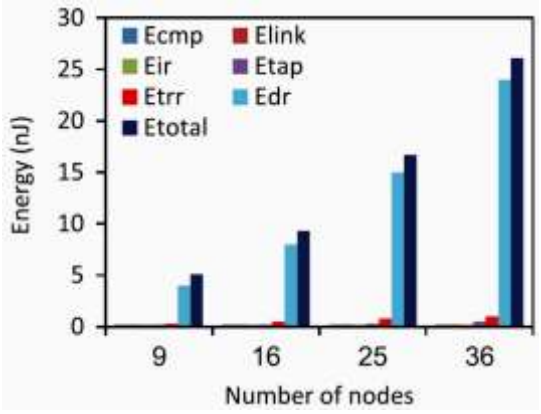


Fig: 7. Result of analysis of several multi core chips in terms of testing energy

As a result, in the next section we are going to propose a low energy high speed circuit-level approach to improve the BSC structure.

The proposed dynamic boundary scan cell

As mentioned, the clock period is a function of DFF delay applied in DR, IR and TRR. One way to enhance the delay is to use dynamic flip flops. Nevertheless, it requires clocking which is energy dissipating. However, looking at the test architecture illustrated in **Figure-1,** shows that a clock is used in order to shift data in shift registers (DR and TRR). Therefore, by reusing this clock, clocking energy overhead can be avoided. Consequently, a special flip flop is designed to be used in JTAG architecture which is depicted in **Figure-7**. In this circuit, two types of latches are used being rising edge triggered (RET) and falling edge triggered (FET). The RET uses only 4 NMOS and 2 PMOS transistors and the FET is designed with 4 PMOS and 1 NMOS transistors as illustrated in **Figure-8**. Then employing master-slave flip flop structure, a DFF is created. According to standard BSC design illustrated in **Figure-3**, UpdateIR, ClockIR, data in signals are connected to the circuit and BSC is constructed. Comparing the current design and the conventional circuit shown in **Figure-9** using static logics, reveals the following point. Firstly, in our design, the number of transistors has been reduced. Secondly by reusing Update IR and Clock IR as clocking signals for dynamic logic, the clocking energy overhead of dynamic logic is significantly decreased. In addition, since in our design, there is no need to invert the clocking signals (Update DR, Update IR, Clock IR and Clock DR), the number of transistors is reduced from 28 in conventional design to 24, which results in even energy reduction.

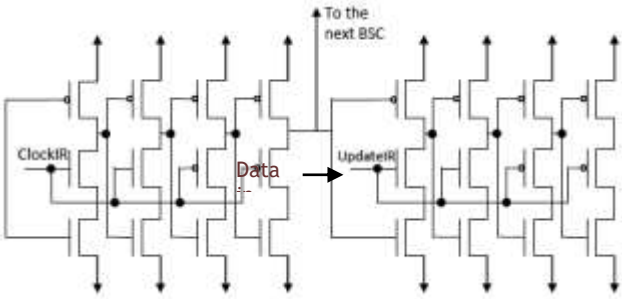


Fig:8.The proposed dynamic design of BSC with 24 transistors

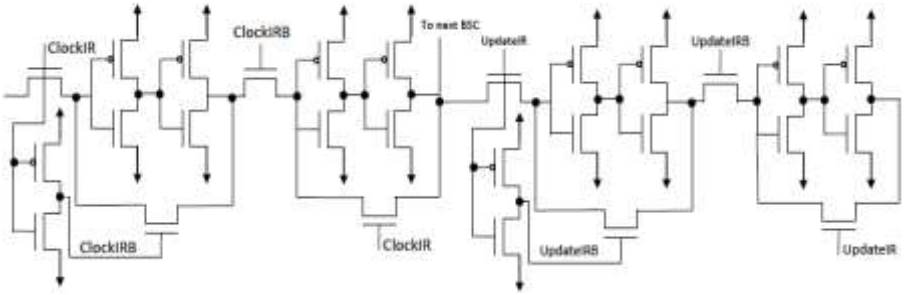


Fig: 9. Conventional design of BSC using static CMOS inverters to implement latches. This design uses 28 transistors

RESULTS

We calculate the energy consumption and test time of the proposed architecture using the presented analytical model. For the basic modules such as flip flops and NAND gates, HSPICE simulation and 32 nm PTM technology model are employed. Table 1, shows the values of HSPICE simulation at 1 V supply voltage, which is the default simulation voltage in this technology. For the output nodes 5 FF output load has been considered which is normal for 32 nm technology. In addition, the energy and delay of the proposed flip flop is compared with those of the conventional static DFF.

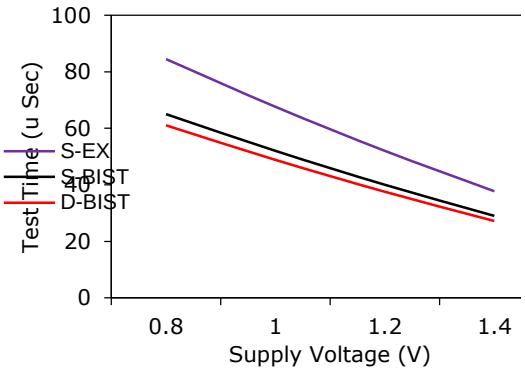
Table: 1. Simulation results for the proposed flip flop, the conventional flip flop and other used gates in the test architecture.

Module	Delay (ns)	EEnergy (fJ)	EDP (fJ.ns)	No. Transistors
Conventional BSC	11.12	0.54	6	28
The proposed BSC	9.34	0.51	4.76	24
2-input OR	3.01	0.102	0.3	6
2input-Nand	2.82	0.093	0.25	4
2-input-Mux	3.12	0.115	0.35	4

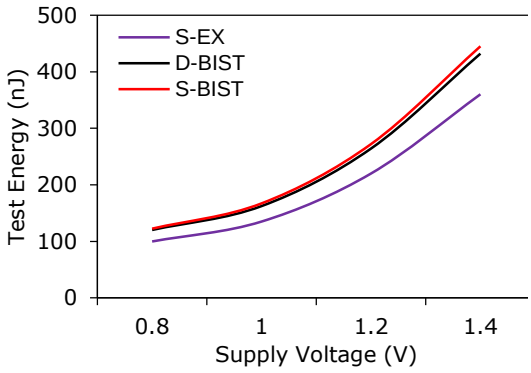
It is seen that the proposed FF has 16% less delay, 5% less energy and 26% less EDP compared to the conventional circuit. The circuit is used in test architecture which is called dynamic BIST (D-BIST) in the results. The test time is seen in **Figure-10(a)** to **10(d)** and energy in **Figure10(e)** to **10(h)**. In this Figure, S-EX, S-BIST are static external tester and static BIST respectively. The proposed architecture has been examined at different conditions of supply voltages in **Figure10(a)** and **10(e),** band widths in **Figure10(b)** and **10(f)**, number of test patterns in **Figure-10(c)** and10(g) and number of no des in **Figure10(d)** and **10(h)**. It is seen that external tester shows at least 29% more delay compared to normal

BIST at different conditions and the proposed BIST shows at least 13 % less delay compared to the normal BIST and 43% compared to external tester at different conditions. Looking at energy, it is found that the energy for the proposed approach is around 4% less compared to that of S-BIST. In addition, it is seen that as the bandwidth, number of nodes, and number of test patterns increases the test time and energy increases as well for all the testing approaches. However, increasing the supply voltage results in decrease in test time while it causes the energy to increases. Since the TPG is located outside the nodes in external tester by increasing the number of nodes the S-EX approach's test time increases exponentially while due to using TPG in parallel in BIST, the test time does not increase too much by increasing the number of nodes. **[Fgure-0(d)]** Increasing the number of nodes however, results in more energy consumption of BIST compared to that of the external tester.

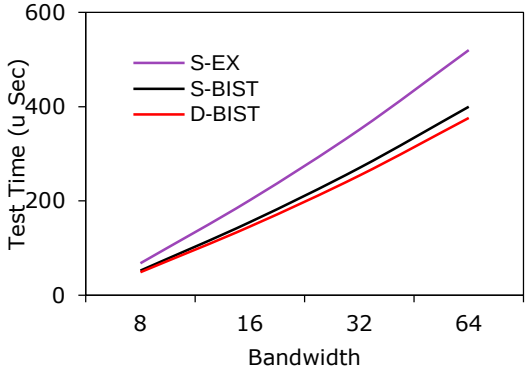
a)



e)

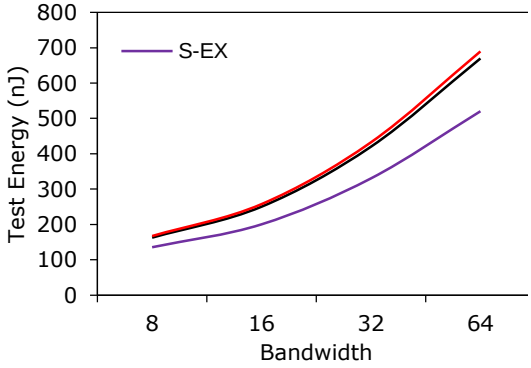


b)



f)

c)



g)

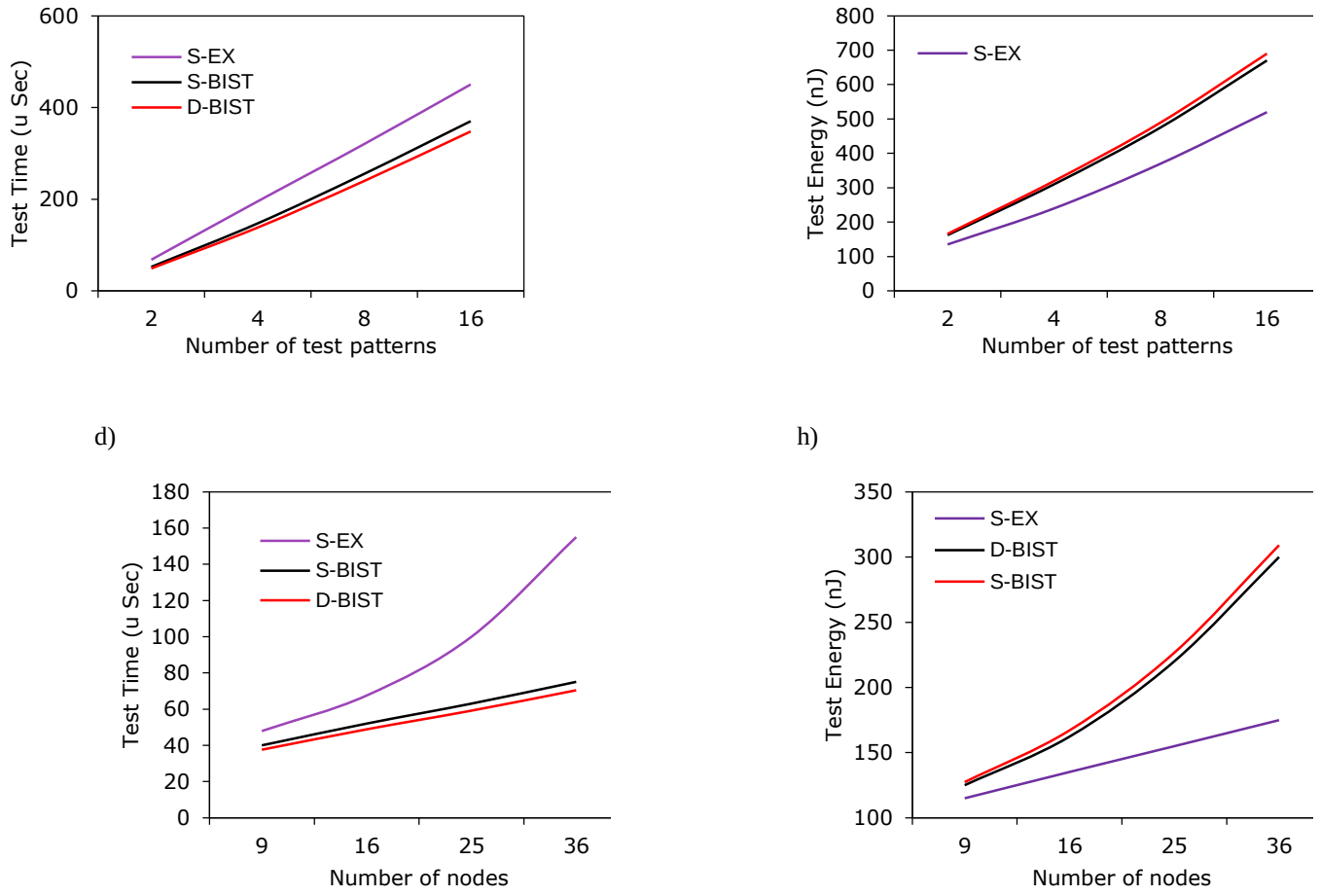


Fig: 10. The result of simulation based on the proposed model for static external tester (S-EX), standard static BIST (S-BIST), and the proposed approach dynamic BIST (D-BIST) at different conditions of supply voltage, bandwidth, number of nodes and number of test patterns. The results show energy consumption and test times of using these approached on NoCs.

CONCLUSION

In this paper, first we proposed a new test architecture for storing test results called test result register (TRR) for application of JTAG in on chip network testing. Using an analytical approach we studied and spotted the critical delay of the built-in self-test (BIST), which found to the boundary scan cells. Standard static BSC used in data register, test result register and instruction registers were replaced by the proposed dynamic BSCs and the JTAG built-in signals were used for clocking the dynamic logics in order to avoid energy consumption overhead of the dynamic logics. Results showed that using the proposed approach due to low transistor count and high speed of dynamic logics, the test time applying BIST was reduced 13% and energy decreased 4% compared to conventional JTAG BIST approach. In comparison to standard JTAG external tester our approach is 43% faster.

CONFLICT OF INTEREST
Authors declare no conflict of interest

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None

FINANCIAL DISCLOSURE
None

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