ISSN: 0976-3104
SUPPLEMENT ISSUE

THE IIOAB JOURNAL
ARTICLE OPEN ACCESS

BLOCK DESIGN ANALYSIS OF CURRENT AND VOLTAGE AC SINGLE-PHASE AND THREE-PHASE INDUCTIVE LOAD IN SIMULINK MATLAB

Mahdi Javaheri* and Masoud Yahyaee

Department of Electrical Engineering, East Tehran Branch, Islamic Azad University, Tehran, IRAN

ABSTRACT

One of the most commonly used in power electronics components are SCR(silicon controlled rectifiers).So there is a need for cognition and work with SCR. Since for analysis SCR should be used Simulink in MATLAB and circuit half control Single-phase to full control three-phase should be implemented in Simulink, In this paper it's written on that.

Published on: 25th– Sept-2016

KEY WORDS

Simulink, Scr, Inductive load

***Corresponding author: Email:** mahdi_javaheri_2007@yahoo.com

INTRODUCTION

In recent years due to the development of the electricity industry in the field of power electronics industry also has a significant progress. With the advent of semiconductor devices and components are used whose structure is based on semiconductors, these devices have earned a special place in power electronics, one of the most practical pieces of equipment SCR, which used as key. The key mechanical motion resulting in longer life and also due to the high speed (about microseconds) One of the benefits this piece is attributed to mechanical keys. After taking into account what was said about the use of SCR had to consider the role of this piece in the converter circuit. As we know in dc to ac or ac to dc converters need to use SCR is controllable with existing drivers to be launched and for purposes of control are required. These circuits are important in power electronics applications and many social, of this converter can be controlled from the bridge or bridge all control three-phase and single-phase all ... named. The first step is to design the circuit in the circuit design is implemented in software environment To the analysis system software bugs and preliminary results discern; One of the most powerful engineering software is MATLAB, Given that in this environment software for circuit simulation in the name of Simulink embedded, MATLAB software into one powerful computing and analytical tools for electrical engineering has become; So be expected if the converter mentioned in the software simulation environment that simulates .Since the simulation of the converter requires the selection of different elements of the library space is Simulink software (and the most important driver of timekeeping is that the process itself);In this paper we shall try the program this converter, together with its drivers to be written (even it can be used as blocks in Simulink library)and Finally, we have to consider its results can Conclude that, by a good percentage desired response is achieved.

METHODS

Electric load

There are 3 types of resistance in alternating current.

Ohmic: The amount depends on the frequency is not a pure ohmic resistance and frequency variations in the amount it is ineffective. The voltage across the resistor R will be displayed as follows.[2,3]

$$u_R=u_m \sin(\omega_t) \qquad (1)$$

THE IIOAB JOURNAL ISSN: 0976-3104

The relationship between flow and the ohmic resistance R passes can be calculated.

$I_R=u_R/R$ (2)

Now in place u_R we putthe same amount that.

$I_R=(u_m \sin(\omega_t))/R$ (3)

$I_R=i=I_m \sin(\omega_t)$ (4)

As can be seen, thedo not have any phase shift between current and voltage.

Induced Reactance: Induced resistance shown by X_L .in Reactance resistance Against ohmic resistance, R is frequency-dependent . X_L Amount obtained from the following equation[1,2]

$X_l=\omega .L$ (5)

According to equation $\omega=2\pi f$ comes to the following equation.

$X_l=2\pi f .L$ (6)

Induced resistance phase shift 90 degree between current and voltage occurs. In other words, the induced resistance Currentis 90 degrees behind from voltage.

2.3-Capacitive resistance: Induced resistance shown by X_c. In Capacitive resistance against ohmic resistance, R is frequency-dependent.[2]

$X_c=1/(c.\omega)$

(7)

Therefore

$X_c=1/(c.2\pi f)$ (8)

Capacitive resistance phase shift 90 degree between current and voltage occurs. In other words, the capacitive resistance Current is 90 degrees forward from voltage.

Because the load on the network are the engine for more power. So ideally all load is of inductance.

SCR

The silicon control rectifier (SCR) consists of four layers of semiconductors, which form NPNP or PNPN structures have three P-N junctions labeled J1, J2 and J3, and three terminals. The anode terminal of an SCR is connected to the p-type material of a PNPN structure, and the cathode terminal is connected to the n-type layer, while the gate of the SCR is connected to the p-type material nearest to the cathode [4]. An SCR consists of four layers of alternating p- and n-type semiconductor materials. Silicon is used as the intrinsic semiconductor, to which the proper dopants are added. The junctions are either diffused or alloyed (alloy is a mixed semiconductor or a mixed metal). The planar construction is used for low-power SCRs (and all the junctions are diffused). The mesa-type construction is used for high-power SCRs. In this case, junction J2 is obtained by the diffusion method, and then the outer two layers are alloyed to it, since the PNPN pellet is required to handle large currents. It is properly braced with tungsten or molybdenum plates to provide greater mechanical strength. One of these plates is hard-soldered to a copper stud, which is threaded for attachment of heat sink. The doping of PNPN depends on the application of SCR, since its characteristics are similar to those of the thyratron. Today, the term "SCR" applies to the larger family of multilayer devices that exhibit bistable state-change behavior, that is, switching either on or off [4]. The operation of an SCR and other SCRs can be understood in terms of a pair of tightly coupled bipolar junction transistors, arranged to cause the self-latching action.

SCR Turn-On

1. forward-voltage triggering
2. gate triggering
3. dv/dt triggering
4. temperature triggering
5. light triggering

Forward-voltage triggering occurs when the anode–cathode forward voltage is increased with the gate circuit opened. This is known as avalanche breakdown, during which junction J2 will break down. At sufficient voltages,

THE IIOAB JOURNAL
ISSN: 0976-3104

the SCR changes to its on state with low voltage drop and large forward current. In this case, J1 and J3 are already forward-biased.

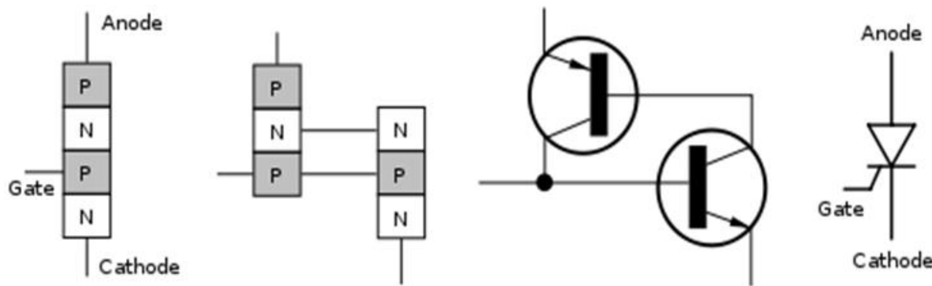

Fig: 1. Schematic Figure and internal structure SCR

SCR Turn-off Transient

When a reverse bias is applied to the SCR anode in order to turn off the device, it is possible to distinguish four separate phases of the ensuing transient: two storage times and two fall times. The device recovers first at the n-emitter junction because there are only very few electrons injected from the wide n base into the Narrow p base. The opposite is true for the n base, since the p base injects heavily into it and replenishes holes as fast as they are collected by the reverse-biased anode. The n-emitter junction breaks down as soon as the junction recovers its depletion region if the applied external potential is high enough. The first storage time and fall time are comparatively short. The second storage time is required to remove the excess charge from the long n base where the holes are continuously replenished by injection by the p base. Finally, all the charge disappears almost at the end of the second fall time. Fast turn offs can be achieved for devices which have low minority-carrier lifetimes (gold doping) and are turned off with high reverse currents. The reverse biasing of the device gate may speed up primarily the first phase of the turn-off transient. If a forward voltage is reapplied prematurely to an unidirectional SCR (SCR) after the forward anode current ceased to flow, the device will go into the conduction state again. Because of the stored charge present, it is necessary to wait for a definite interval of time after current cessation before the Reapplication of the forward potential if the device is expected to block the reapplied voltage. The turn-off time is the time necessary for the removal of the excess charges from all the parts of the p-n-p-n device. In many practical applications the forward current is removed from the SCR by the reversal of the current flow in the outside circuit; the decreasing anode current passes through zero and goes negative. It has its maximum value just after the reversal and decays until all the excess charges are removed and a depletion layer has fully developed across the reverse-blocking junction. Only then is the SCR ready for the reapplication of the forward potential. Generally speaking, the device can be turned off not only by the application of a reverse potential but also by opening the external circuit or by applying a reverse bias to the device gate. The most rapid turn-off is achieved when the anode current is reversed with simultaneous reversal of the gate current. We consider first the case when the anode current only is reversed; consequently, the two outer junctions, which were forward biased during the on state, become eventually reverse biased. The effect of the additional application of the reverse gate current is shown, then, to decrease the turn-off time. The device behavior can be analyzed one-dimensionally by the charge-control method using the superposition principle [5-8].The results of the one-dimensional analysis are applicable obviously with greater accuracy to structures with narrow emitters.

THE IIOAB JOURNAL
ISSN: 0976-3104

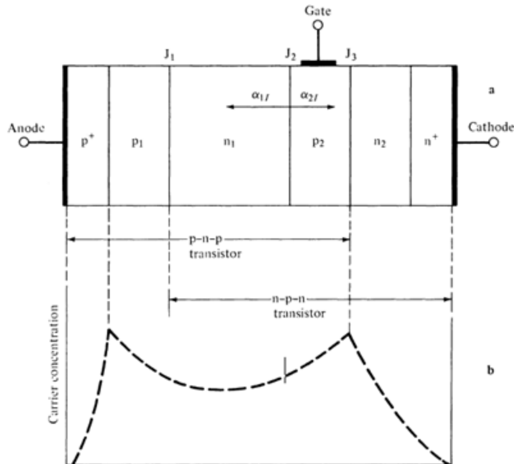

Fig: 2. An SCR and an approximate carrier concentration at *t* = O

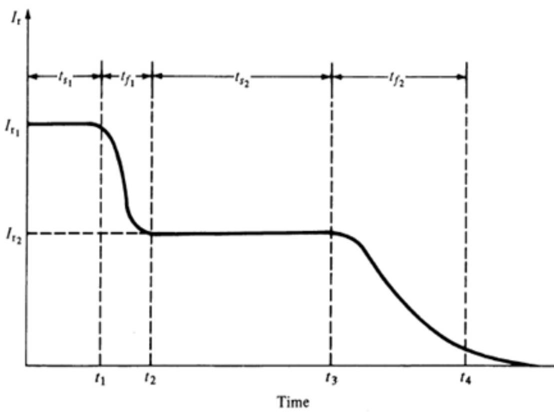

Fig: 3.Four turn-off phases [7].

[Figure- 8.1] represents a p-n-p-n device just prior to the application of the reverse potential to the anode. For the reverse-bias turn off, the current waveform may be divided into four regions corresponding to the four turn-off phases [Figure- 3].

Storage time(t_(s_1))

The n base in a power device is usually uniformly doped with very low impurity concentration (~〖10〗^14 atoms/cm3 or less). Thep base, on the other hand, is doped no uniformly and may have an average impurity concentration on the order of 5×〖10〗^15 atoms/cm3. As a result, in the forward-blocking state when the center junction J2 is forward biased and injecting, its emitting efficiency is good from the p base into the n base, but very poor in the opposite direction. For this reason, the turn off of the p-n-p-n device starts with the removal and decay of excess minority-carrier concentration (electrons) from the p base when the n-emitter efficiency is high. The reverse-biased cathode (positive) has to collect only the charges (electrons) present in the p base which are hardly replenished by the injection from the n base. It is not so in the n base, since as soon as the charges (holes) are collected by the reverse-biased anode (negative), more holes are injected efficiently by the p base into the n base. Consequently, the turn off starts with the n-emitter junction J3.During the t_1 [Figure-3] the current through the device is constant because there is a large charge stored in the p base which allows the current to flow when the bias is reversed. As long as the excess charges are not entirely removed from the p-base junction, J3 will remain forward biased despite the external voltage reversal. Neglecting the forward voltage drop across the device, the constant Current through the device during t_1 equals.

THE IIOAB JOURNAL ISSN: 0976-3104

$I_{r_1} = v_r/R$ (9)

Where V_r. is the reverse voltage pulse amplitude and R is the circuit resistance (ohmic load is assumed).At the end of the time t_1, enough electrons are removed by the reverse (positive) potential applied to the cathode, the depletionregion of the J3 junction begins to widen, and J3 starts supporting the reverse bias [5-7].Using charge-storage relationships, it is possible to obtain the following expression for the first storage time (notation as per **Table- 1 and Figure- 2]**:

$t_{s_1} = \tau_2 \ln[(\gamma_{1I} I_{r1} + A_P I_F)/((1-\alpha_{2I}) I_{r1})]$ (10)

$\alpha_{2I} = \beta_{2I} \gamma_{2I}$ (11)

Where I_F is the on-state current, A_P is a constant, τ_2 is the lifetime in the p-base, γ_{1I} is the emitter efficiency of the p2-nl-p1 transistor, α_{2I} is nl-p2-n2 transistor DC gain, β_{2I} is the nl-p2-n2 transistor transport factor, and γ_{2I} is thenl-p2-n2 transistor emitter efficiency. For $\alpha_{2I} \gg 1$ and $\gamma_{1I} \approx 1$, this expression reduces to a simple relationship

$t_{s_1} = \tau_2 \ln(1 + A_P I_F/I_{r1})$ (12)

Thus, the first storage time can be made small if the lifetime in the p- base is short and/or the reverse current is high.

Fall time (t_{f_1})

There are two possible situations that should be considered: (1) the n-emitter junction recovers, i.e., its depletion region builds up, but the externally applied voltage is smaller than the junction breakdown voltage; and (2) the applied voltage is large enough to cause the breakdown of the n-emitter junction J3 (or the n emitters shorted).

Table 1:
Notation used for the turn-off transient analysis

Parameter	n_2-p_2-n_1 transistor	n_1-p_2-n_2 transistor	p_1-n_1-p_2 transistor	p_2-n_1-p_1 transistor
Common base DC current gain	$\alpha_N = \gamma_2 \beta_2$	$\alpha_{2I} = \gamma_{2I} \beta_{2I}$	$\alpha_P = \gamma_1 \beta_1$	$\alpha_{1I} = \gamma_{1I} \beta_{1I}$
Transport factor	β_2	β_{2I}	β_1	β_{1I}
Emitter efficiency	γ_2	γ_{2I}	γ_1	γ_{1I}
Base transit time	T_2	T_{2I}	T_1	T_{1I}
Minority-carrier lifetime in the base	τ_2	τ_2	τ_1	τ_1

Letter I is used for inverse parameters **[Figure- 2]**.

In the first case it was shown by Sundresh [7] that the decaying current has the for

$I(t) = (K_1 \tau_2)/T_{2I} \; I_{r1} \exp((-t)/\tau_2)$ (13)

With

$K_1 = \gamma_{2I}(1-\beta_{2I})$ (14)

and the origin for time is assumed to be at the end of t_{s_1}; T_{2I} is the minority carriers' (electrons) transit time in the p base in the inversedirection from the n base toward the n emitter. when there is no breakdown, the expression (12) permits the determination of the first fall time. The second case in which breakdown occurs is usually more important from the practical point of view and corresponds to high-node reverse-applied potentials. For this case [7]

$t_{f_1} = \tau_2 \ln[\tau_2/T_{2I} \; \gamma_{2I}(1-\beta_{2I})(I_{r1} R)/(I_{r1} R - V_B)]$ (15)

V_B is the n-emitter (junctionJ3) breakdown voltage. The requirements for the short fall time t_{f_1} are: small minority-carrier lifetime in the p base, low breakdown of the n-emitter junction, and low injection efficiency from the n base into the p base.

5.3. Storage time (t_{s_2})

As the voltage reaches the avalanche breakdown of the n-emitter junction J3, the voltage drop across J3becomes constant and remains in series with the rest ofthe device which consists of the p-n-p portion still conducting fully and contributing a negligibly small voltage drop. As soon as J3 breaks down, a second storage time starts, during which the current remains essentially constant and can be determined from.

$I_{r_2} = ((V_r - V_B))/R$ (16)

THE IIOAB JOURNAL ISSN: 0976-3104

The center junctionJ2 is a good emitter of holes and an inefficient emitter of electrons so that the hole injection into the n base from J2will continue as long as J2 is forward-biased. The n base recovers then more slowly than the p base because of this continuous replenishment of holes. Using the charge-control method, it is possible to obtain a simple expression for t_{s_2}. If we assume for simplicity that. the fall time τ_{f_1} is negligibly small and both emitters (n and p) have unity gamma, then for high-anode reverse-bias

$$t_{s_2} = \tau_2 \ln\left(C_1 + C_2 \frac{I_f}{I_{r_2}} \right) \quad (17)$$

where C_1 and C_2 are algebraic functions of the normal- and reverse-current gains[5]. Here again, large reverse current and short minority-carrier lifetime in the n base will reduce the duration of the storage time.

5.4. Fall time (t_{f_2})

Assuming that the carrier flow during this phase is by diffusion only and that the charge distributions in both bases are linear, it is possible to obtain an analytical expression linking the currents to the charges in each base [7]. In power SCRs we have usually $\gamma_{2I} \gg \gamma_{1I}$ and the current during the second decay time may be expressed by

$$I(t) = I_{r_2} \tau_1 \gamma_{1I} (1-\beta_{1I}) \frac{1}{T_{1I}} \exp\left(\frac{-t}{T_{1I}}\right) \quad (18)$$

where τ_1 is the lifetime in the n-base, β_{1I} is the p_2-n_1-$p_1$transistortransport factor, and T_{1I} is the p_2-n_1-p_1 transistor base transit time. The fall time t_{f_2}can be determined from (18) by letting the current$I_{(t)}$drop down to the holding current level; for instance,

$$t_{f_2} = T_{1I} \ln \frac{I_{r_2} \tau_1 \gamma_{1I} (1-\beta_{1I})}{I_h T_{1I}} \quad (19)$$

The second fall time can be decreased by short minority-carrier lifetime in the n base and short inverse transit time.

The same data show the direct proportionality of the saturation times to theminority-carrier lifetimes in respective device bases The circuit commutated turn-off-time T_q measurements! confirm essentially the validity of the above theoretical considerations in so far as the total switching time is concerned, since$T_q$behaves qualitatively in the same way as switching time $t_{s_1}+t_{s_2}+t_{f_1}+t_{f_2}$.

RESULTS

Real waveform Simulink

The following Simulink we see controlled half-wave circuit that in the 2 stage is tested.In step 1, inductance load is 2 H and step 2 changes to 5 H. Results are as follows.m[**Figure-4a-4e]**.

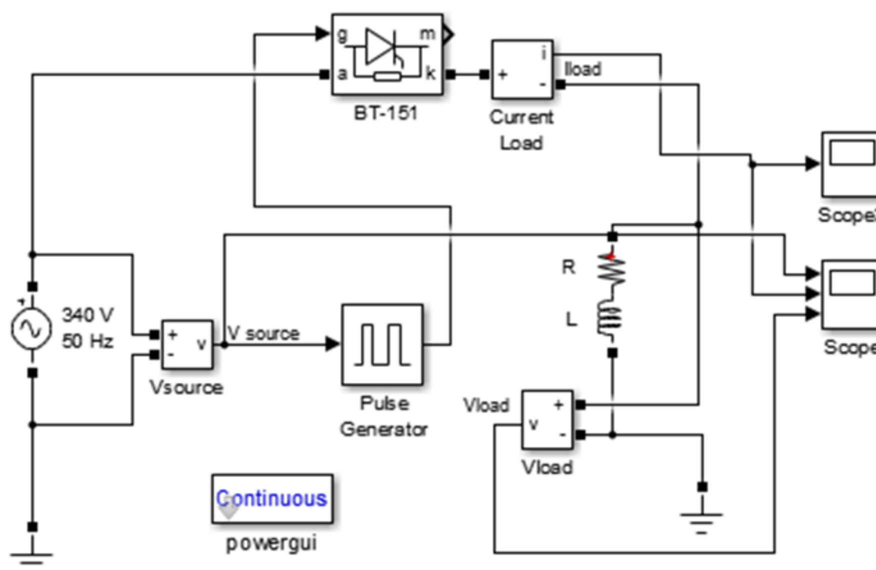

Fig:(4a). Simulink

………..

THE IIOAB JOURNAL
ISSN: 0976-3104

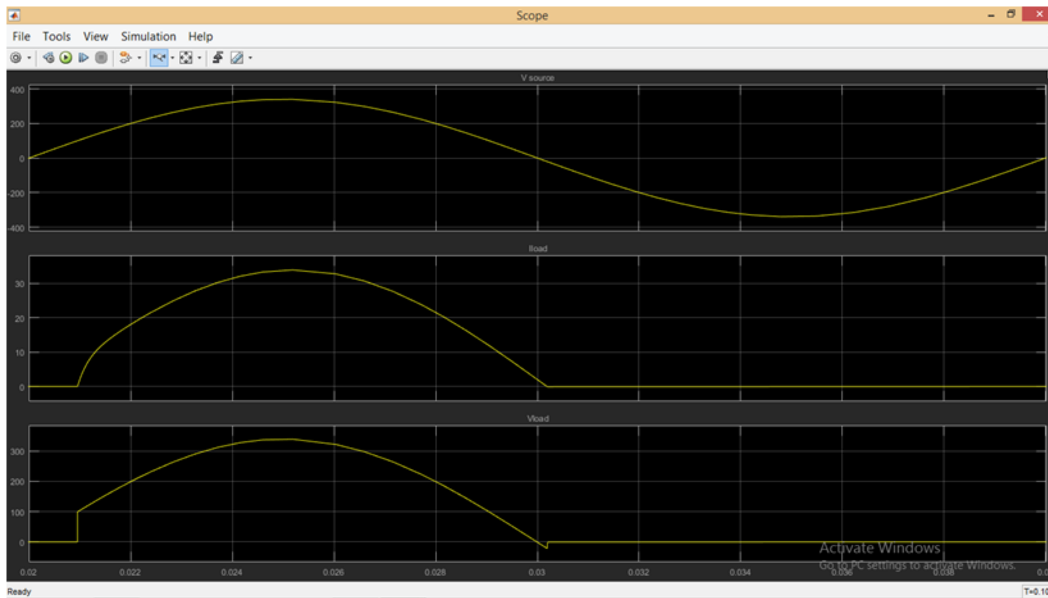

Fig: 4(b).Real Simulink Waveform(V source, I load, V load)Load inductance=2H

…….

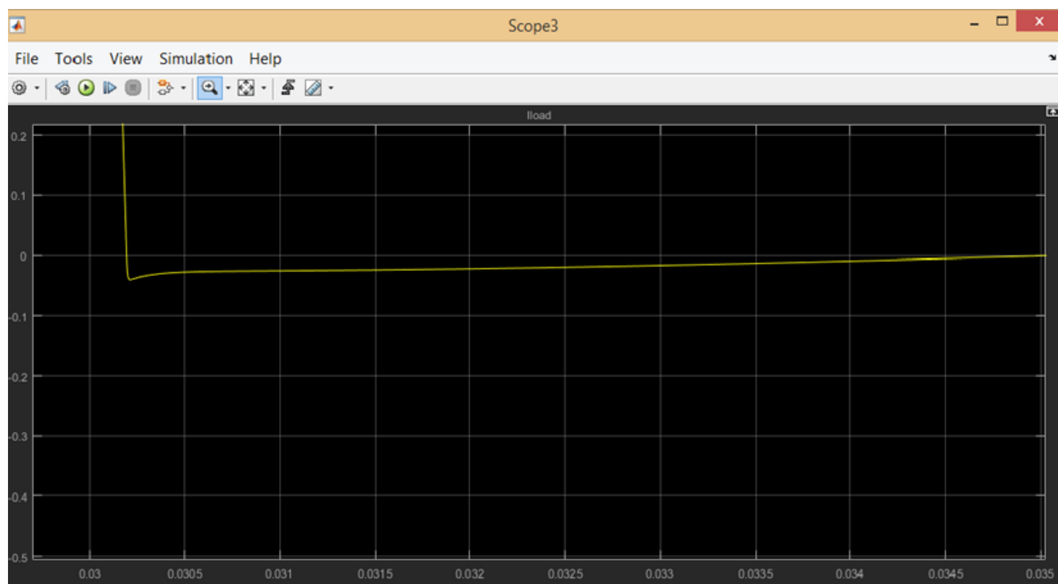

Fig: 4(c).I load (Detailed View) Load inductance=2H

…….

THE IIOAB JOURNAL ISSN: 0976-3104

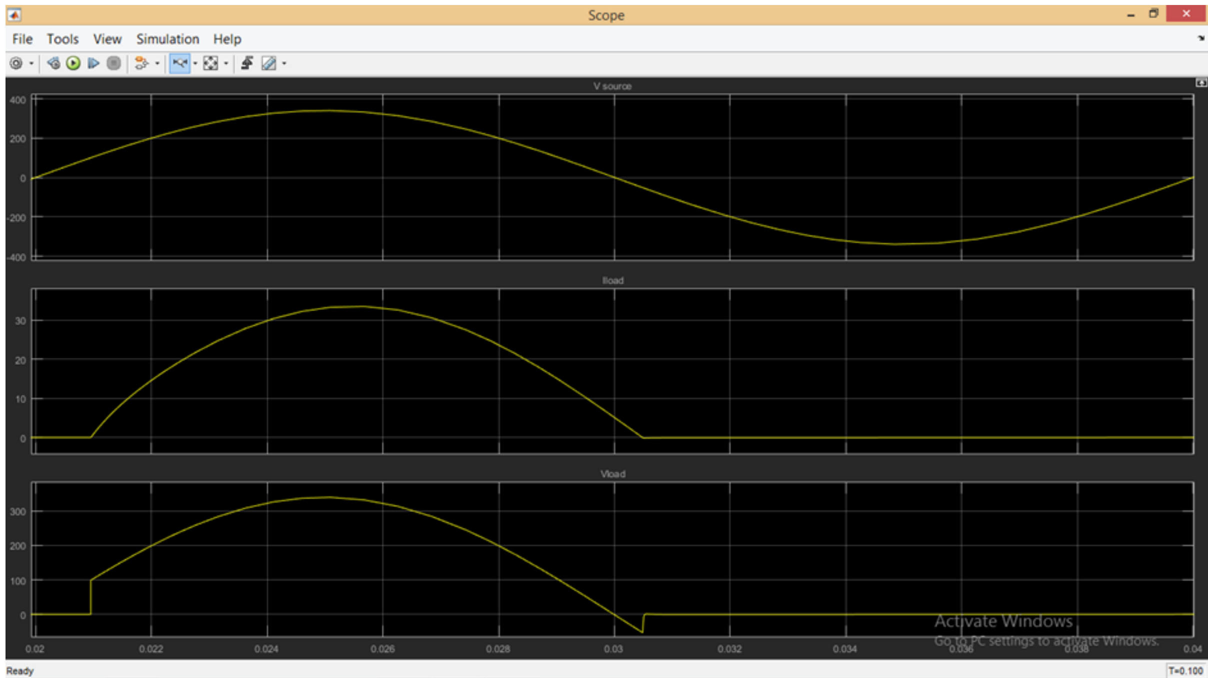

Fig: 4(d). Real Simulink Waveform(V source, I load, V load)Load inductance=5H

………

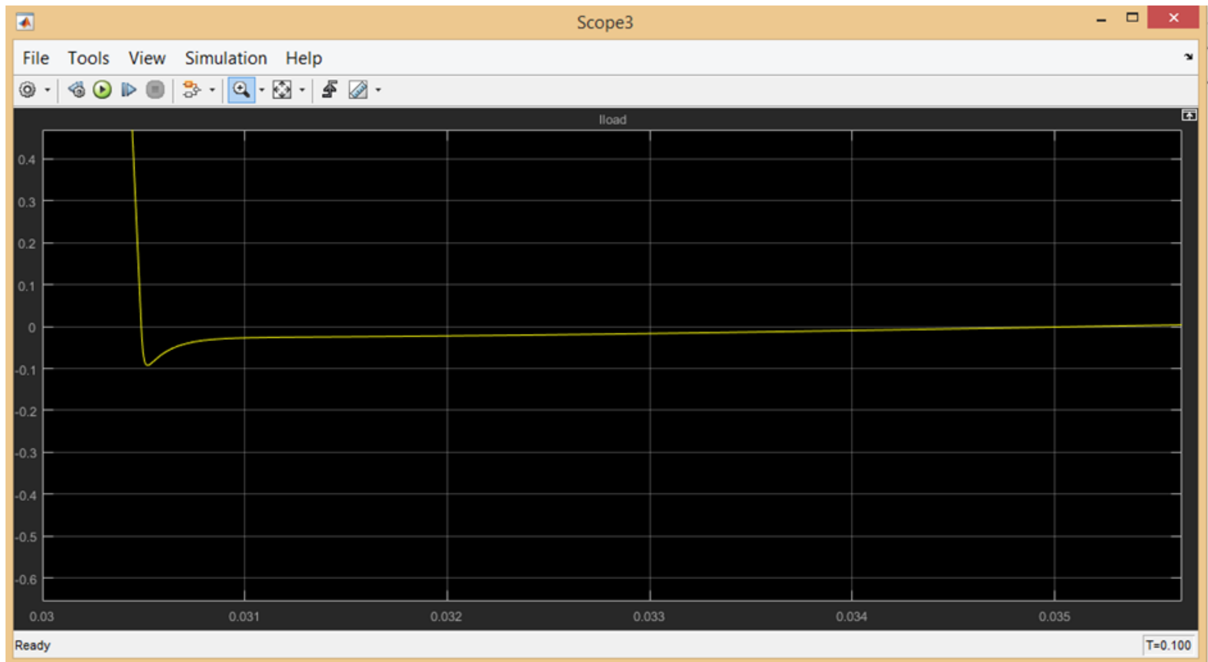

Fig: 4(e).I load (Detailed View)Load inductance=5H

………

Result program (main Result)

Based on the above explanation wrote the following program The following parameters related to certain intrinsic is a SCR BT-151 which has been extracted from the data sheet.

THE IIOAB JOURNAL ISSN: 0976-3104

V_B=500(n-emitter (junction j3) breakdown voltage: 500 v)
I_h=.007(I_h=7mA-20mA)
A_P=1(constant: 1)
I_f=.012(on-state current: 12mA)
τ_1=5$\times 10^{-9}$(lifetime in the p-base: 5 ns)
τ_2=3$\times 10^{-9}$(lifetime in the p-base: 3 ns)
β_{1I}=.5(transport factor of the p2-n1-p1 transistor: 0.5)
β_{2I}=.2(transport factor of the n1-p2-n2 transistor: 0.2)
T_{1I}=.02(minority carrier transit time Tr p2-n1-p1: 20 ms)
T_{2I}=.05(minority carrier transit time Tr n1-p2-n2: 50 ms)
I_{r_1}=1(emitter efficiency of the p2-n1-p1 transistor: 1)
I_{r_2}=.5(emitter efficiency of the n1-p2-n2 transistor: 1)
C_1=1(reverse current gain: 1)
C2=1.1(reverse current gain: 1.1)

Single-phase half-wave:

In the first case(State1) the data resulting waveform to see،The impact waveform is specified inductance inductive load .Now the program written to show the influence of the inductance of the inductive load will change its value from 2 to 5(State2), As to the effect of the inductance of the load on the current and voltage circuit was explained, In the second case, clearly the impact of the inductance waveform in the waveform turns out to be, So we can verify the correct operation of the written application accepted.**[Figure-5(a) to 5(d)]**

State1:
PeakV input=340
Frequency input=50
Load inductance input=2
Load Resistance input=10
Firing angle input=30

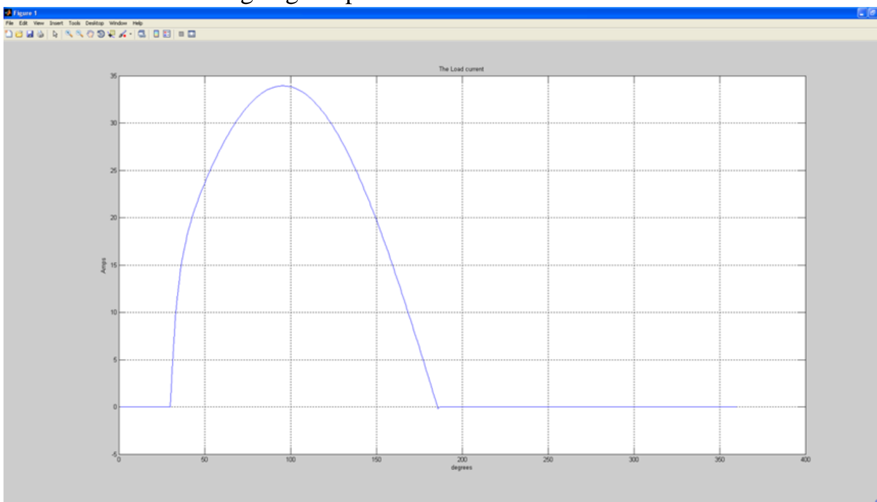

Fig:5(a).Result Waveform (Load current)

……

THE IIOAB JOURNAL ISSN: 0976-3104

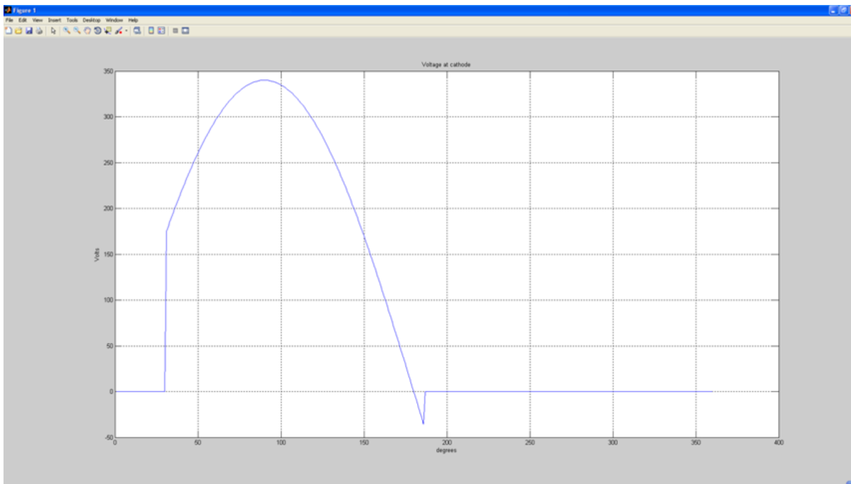

Fig: 5(b):Result Waveform (Load Voltage)

....

State2:

PeakV input=340

Frequency input=50

Load inductance input=5

Load Resistance input=10

Firing angle input=30

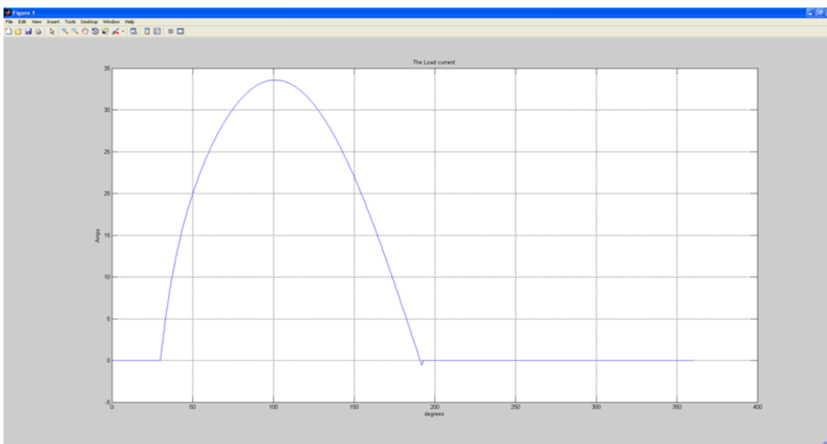

Fig:5(c):Result Waveform (Load current)

....

THE IIOAB JOURNAL
ISSN: 0976-3104

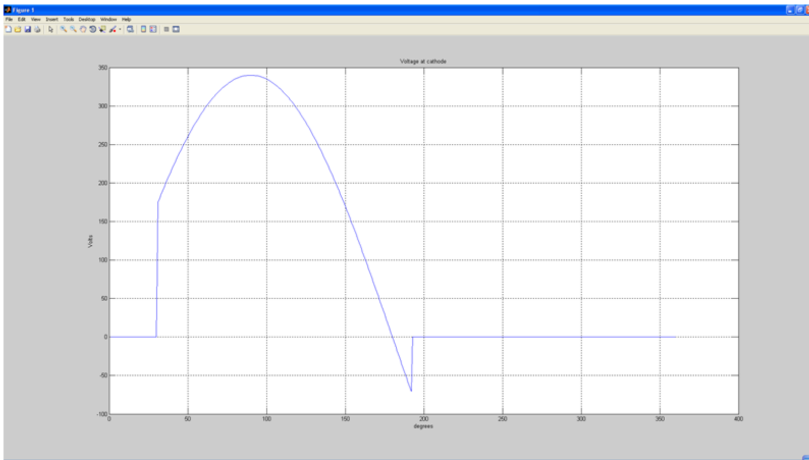

Fig: 5(d). Result Waveform (Load Voltage)

……

Single-phase full-wave:

A half-wave rectifier waveform in the following models can be viewed with inductive load.Figure(6)

PeakV input=340
Frequency input=50
Load inductance input=2
Load Resistance input=10
Firing angle input=30

Waveform Voltage

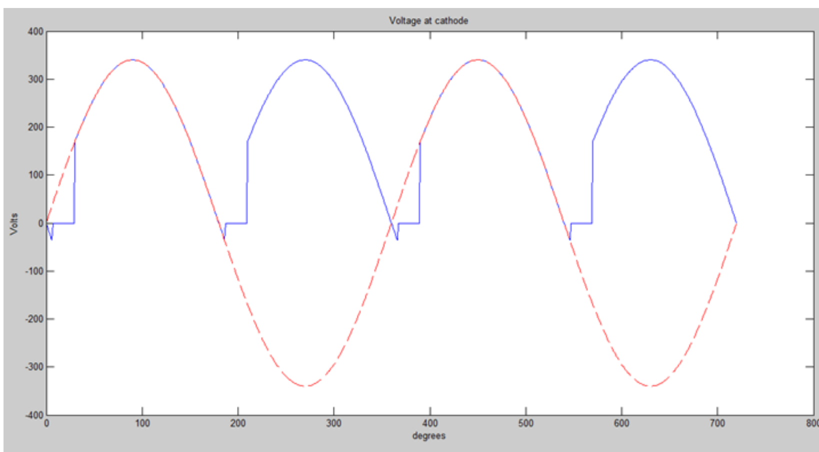

Fig: 6.Waveform Voltage Single-phase half-wave

…….

phase full-wave:

A 3-phase full-wave rectifier waveform in the following models can be viewed with inductive load.Figure(7)

PeakV input=340
Frequency input=50

THE IIOAB JOURNAL ISSN: 0976-3104

Load inductance input=2
Load Resistance input=10
Firing angle input=30

Waveform Voltage

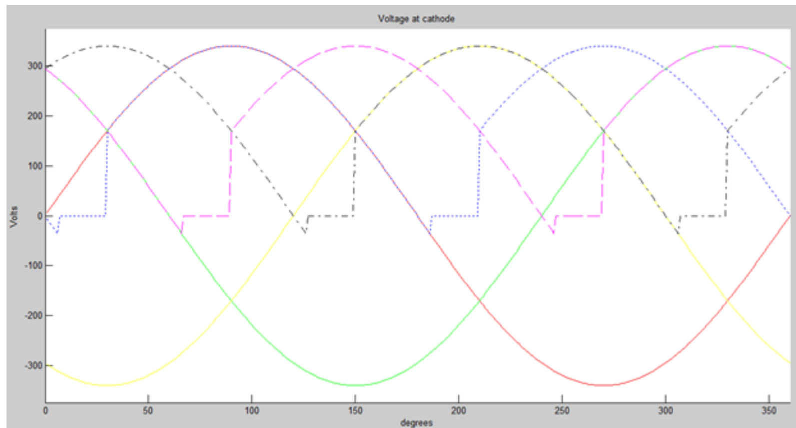

Fig: 7. Waveform Voltage 3-phase full-wave

CONFLICT OF INTEREST
Authors declare no conflict of interest

ACKNOWLEDGEMENTS
None

FINANCIAL DISCLOSURE
None

REFERENCE

**DISCLAIMER: *This is uncorrected proof. Plagiarisms and references are not checked by IIOABJ.*

[1] Electrical Machines, Drives, and Power Systems, 4th edition, Theodore Wildi, Prentice Hall, ISBN 0-13-082460-7, pages 311–314.
[2] Rajendra Prasad. [2006] Fundamentals of Electrical Engineering. Prentice-Hall of India. ISBN 978-81-203-2729-0
[3] James William Nilsson and Susan A. Riedel (2008). Electric circuits. Prentice Hall. p. 29. ISBN 978-0-13-198925-2.
[4] Christiansen, Donald; Alexander, Charles K. (2005); Standard Handbook of Electrical Engineering (5th ed.). McGraw-Hill, ISBN 0-07-138421-9
[5] Baker AN, Goldey JM, Ross IM. Recovery time of PNPN diodes, 1959 IRE Wescon Convention Record, Part 3: 43-48.
[6] Gentry RE, Gutzwiller FW, Holonyak N, Von Zastrow Jr. EE.[1964] Semiconductor Controlled Rectifiers. Englewood Cliffs, N.J.: PrenticeHall.
[7] Sundresh TS. [1967]Reverse transient in PNPN triodes. *IEEE Trans. Electron Devices*, 14: 400-402
[8] Davies RL and Petruzella J.[1967] PNPN charge dynamics. Proc. *IEEE,* 55 (8): 318-330.