IIOAB JOURNAL
ISSN: 0976-3104

ARTICLE

DESIGN AND IMPLEMENTATION OF PIPELINED RADIX-2 SDF-SDC FFT USING MODIFIED CARRY SELECT ADDER

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ABSTRACT

This paper presents the design of power efficient structures of Radix-2 Decimation in Frequency (DIF) pipelined butterflies, aiming the implementation of high speed and low power Fast Fourier Transform (FFT) using modified carry select adder. In the traditional method of FFT, the processing speed is low and large power consumption. So, the pipelined SDF-SDC FFT using carry select adder has been designed. Compared to traditional method, the pipelined SDF-SDC using carry select adder is used to reduce the power consumption. The main goal of this paper is to reduce the hardware slices, LUTs, delay and power consumption. In this paper, we modified the carry select adder by reducing the full adder structure to reduce the hardware slices, delay and power consumption. "Pipelined radix-2 SDF-SDC FFT using modified carry select adder" has been proposed in this paper. The Full adder circuit is shrunk down by reducing number of gates. Finally, the modified carry select adder circuit is integrated into SDF-SDC FFT processor. When compared to traditional equivalents, the proposed architecture which is used to improve the high processing speed and high performances of FFT processor. By using modified carry select adder the FFT processing time is reduced and also the speed can be improved. Simulation of proposed Radix-2 SDF-SDC FFT using modified CSLA architectures are evaluated by using ModelSim 6.3C and performances are validated by using Xilinx ISE10.1 design tool.

KEY WORDS
Single path Delay Commutator, Carry Select adder, Decimation in Frequency, Fast Fourier Transform, Single path Delay Feedback, Look Up Tables

Received: 25 Aug 2016
Accepted: 2 Sept 2016
Published: 12 Sept 2016

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INTRODUCTION

Fast Fourier Transform (FFT) is the largely implementation of the Discrete Fourier Transform (DFT) used in some communication systems PHY layer and DSP. This algorithm performs the calculation of complex terms, which involves the multiplication of input data by appropriate coefficients. The FFT algorithm, started a new era in digital signal processing by reducing the orders of complexity of DFT multiplications compared to a normal DFT. Since multipliers and adders are very power hungry elements in VLSI designs they result in consequent power consumption. The basic principle of FFT is that to find mechanism of time saving. The Fast Fourier Transform analysis is to convert the original signal to frequency domain signal and vice versa.

We need to perform N multiplications and N-1 additions for an N-point DFT. Therefore, there will be complex multiplications of N2 and complex additions of N (N-1). Different platforms such as computer chips and general purpose processors are implemented by the Fast Fourier Transform (FFT).FFT uses a divide and conquer methodology for its computation process. This divides the N co-efficient into smaller blocks in different stages.

Adders are mostly used in electronic applications. Digital adder is an important specification in advanced digital processors for faster computation. The speed of addition is limited by the time needed for a carry to propagate through the adder, in digital adder circuits. Adders in circuits acquire extremely large area and consume large power as large additions are finished in advanced systems. Adder is one of the important blocks in ALU and DSP systems. An adder plays a significant role include convolution, digital filtering like DFT, FFT, digital communications and spectral analysis.

In the traditional FFT which uses the adder structure is not suitable due to its low processing speed and large power consumption. Here, the traditional adder is replaced with proposed carry select adder. In this paper, pipelined radix-2 SDF-SDC FFT using modified carry select adder is used to high processing speed and high performances of FFT processor.

LITERATURE SURVEY

[1] Explained the design of pipelined structure from Radix-2 FFT with DIT algorithm using efficient adder compressors. The different and dedicated structures for the 16 bit-width pipelined radix-2 DIT butterfly running at 100MHZ are implemented. The main goal of this paper is to minimize the number of real multipliers of the architectures. This is done by varying the structure of the complex multipliers and applying them into the butterflies. The adder compressors structures are widely used in fast and low power multiplier architectures. Parallel FFT processor has more disadvantages in hardware utilization and speed of processing. In order to overcome the problem of parallel FFT, Pipelined FFT processor such as R2SDF and R2MDC FFT structures has been introduced in [2]. In [2], Pipelined Radix-2k FFT structures have been developed with the help of Feed forward structures. Feed forward structure provides 26ns for performing 8-point FFT.

ISSN: 0976-3104

[3] Explained the FFT processor using radix-24 feed forward pipeline architecture, which has low latency, high throughput and lesser area. In FFT computation, there are number of complex multiplication and addition operations. In VLSI implementation of FFT, multipliers takes large time in calculation, therefore it increases the delay of FFT processor.[4] Described the efficient combined single-path delay commutator-feedback (SDC-SDF) radix-2 pipelined FFT architecture, which includes N number of sdc stages and 1 SDF stage. The combined SDC-SDF pipelined FFT architecture which provides the output data in the normal order. The SDC processing engine is to achieve 100% utilization. The proposed SDC PE reduces 50% complex multipliers, compared with other radix-2 FFT.

[5] Explained the CS operation is scheduled before the computation of final-sum, which is different from the traditional approach. Carry words identical to input-carry '0' and '1' generated by the CSLA based on specific bit pattern, which is used for logic optimization of the CS unit. For logic optimization, fixed input bits of the CG unit are also used. An optimized design for CS and CG units are obtained. An efficient design is obtained for the CSLA, by using these optimized logic units. CSLA design involves less area and delay than the BEC based CSLA.[6] described the new design of LPPL FFT processor and its two basic building blocks, butterfly in pipeline and address generator.[7]-[9] explained an efficient adder design essentially improves the performance of a complex DSP system.[8]-[10] presented the low-cost VLSI implementation of a pipeline fast fourier transform capable of supporting from 1k to 32k FFT sizes.

RADIX-2 FFT STRUCTURES

Radix-2 FFT algorithm retaining to divides the N-point DFT into two N/2 point DFTs and a complex multiplication in between.The DFT of N-point time domain signal is represented by

$$X_k = \sum_{n=0}^{N-1} x_n W_N^{nk}$$

0≤k≤N-1

Where, Xk is the DFT (frequency) representation of discrete signal xn, W_N^nk denotes the twiddle factor and N represents the
Number of points.

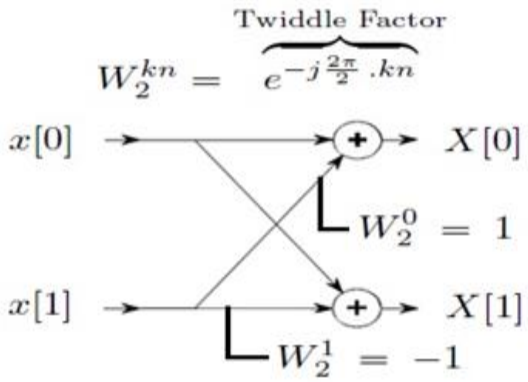

Fig. 1: Structure of Radix-2 FFT

Radix-2 FFT algorithm calculates the FFT in following three levels a) Decompose an N-point time domain signal into N number of separate signals such that each consists of a single point. It is a multistage interlaced decomposition where odd indices and even indices get separated. b) Calculate the N frequency spectra corresponding to N time domain signals. c) Synthesize the resulting N number of spectra into a single frequency spectrum.Radix-2 FFT consists of two types, one is Decimation in Time (DIT) FFT and next one is Decimation in Frequency (DIF) FFT. Input bits are given in reversing order and output is obtained as normal order, in DIT FFT. But in DIF FFT, input is given to normal order and the output is obtained as bit reversing order.

EXISTING METHOD

Single path Delay Feedback – Single path Delay Commutator (SDF-SDC) FFT

The SDF FFT is a serial processor which provides high speed operation. In R2SDF, the inputs are given into serial manner. In R2SDF FFT, N/2 point input data is sequentially controlled with the help of Flip-Flop circuit. This FFT structure consumes more number of hardware utilization and power consumption due to

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ISSN: 0976-3104

utilizing or storing bulk of unwanted intermediate processing signals. Hence, large power consumption is one of the main disadvantages of R2SDF FFT. Single Path delay Commutator FFT has more number of single delay commutators within one stage. But in case of SDF FFT, single number of large delay feedbacks is used to implement the functions of FFT. Both SDF and SDC architectures are used in the proposed design. In the place of multiplier unit, Bit Parallel Multiplier is used for multiply the subtracted data into corresponding twiddle factor values. Complex input data is considered to perform the FFT function. In every step, there is single delay commutating function has been used to process the appropriate data points. The Multiplexer units have been used to provide control signals for performing Commutator functions. Further signed addition and signed subtraction units are used to perform accumulation and subtraction functions. When compared to SDF structure, SDC architecture has more computational paths to perform FFT function. Hence, to improve the architectural performances of FFT combined Single-path Delay Feedback (SDF) – Single-path Delay Commutator (SDC) FFT architecture has been designed in this paper. This achievement can be obtained due to sharing or utilizing 50% of same hardware resources for computing multiple functions. The architecture of 16 point SDF-SDC FFT is illustrated in [Fig. 2].

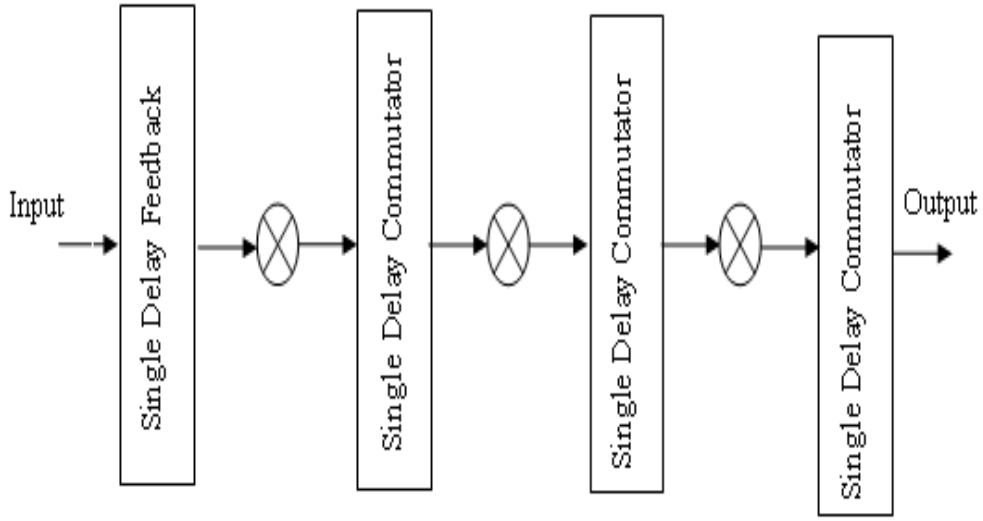

Fig. 2: Architecture of 16 point SDF-SDC FFT

Carry Select Adder

A carry select adder is a combinational logic of arithmetic circuit, which adds the binary value of 2 N-bit numbers and outputs their N-bit binary sum and a 1-bit carry. Carry select adder comes in the group of conditional sum adder. Sum and carry are computed by assuming input carry as 1 and 0 prior the input carry comes.

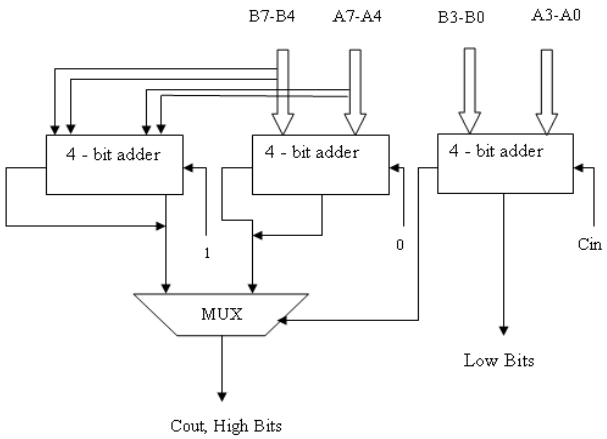

Fig.3: Architecture of Carry Select Adder

ISSN: 0976-3104

When the input value of carry arrives, the actual calculated values of sum and carry are selected using a multiplexer. In the FFT processor, the computational procedure includes vast number of multiplications and additions. To implement the addition operation in the FFT processor, carry select adder has been used. In the existing method of SDF-SDC FFT using carry select adder, which is used to reduce the power consumption of the FFT processor. The architecture of Carry select adder is illustrated in [Fig.3].

PROPOSED METHOD

Modified Carry Select Adder

In the carry select adder circuit, full adder circuit is reduced to improve the performances of the structure. Full adder is the important block of CSLA circuit. The carry select adder circuit consists of 4-bit adder (4 Full adders) and multiplexer. The reduced full adder design has been illustrated in this section.

Reduced Full Adder

Full Adder circuit has been realized and redundant functions are eliminated to improve the architectural performances. The generalized Full Adder circuit block is illustrated in [Fig. 4]. FA circuit consists of two XOR gate, two AND gate and a single OR gate to perform the 3-bit addition operation. Reduced Full Adder (RFA) circuit has been designed by using minimal number of logic gates. Also Multiplexer (MUX) based RFA circuit has been designed in this paper to further alleviates the performances of digital adder circuits.

Gate Count of Full Adder is determined as follows,
Gate Count of FA = Gate Count [(2*XOR) + (2*AND) + (1*OR)]
Gate Count of FA = [(2*5) + (2*1) + (1*1)] = 10+2+1 = 13
Gate Count of Reduced Full Adder = Gate Count [(2*AND) + (1*OR) + (2* NOT) + (1*MUX)]
Gate Count of Reduced Full Adder = [(2*1) + (1*1) + (2*1) + (1*4)] = 2+1+2+4 = 9
The structure of Reduced Full Adder (RFA) is illustrated in [Fig.5].

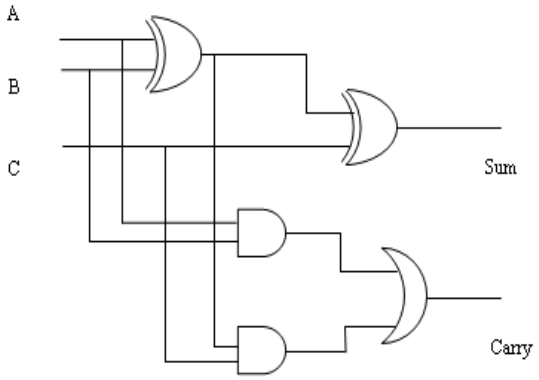

Fig. 4: Full Adder Circuit

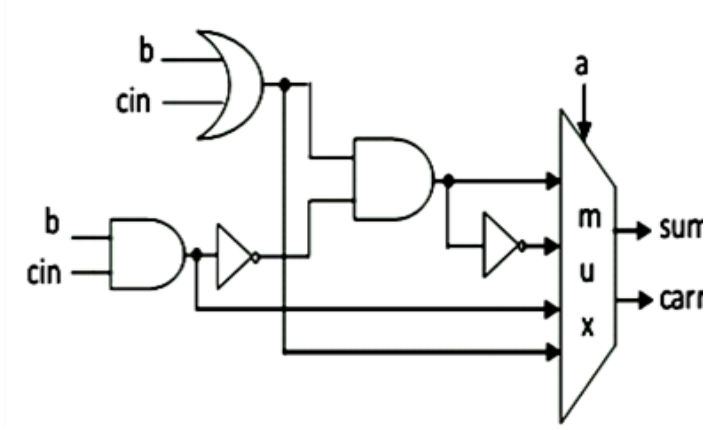

Fig.5: Reduced Full Adder Circuit

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ISSN: 0976-3104

Pipelined Radix-2 SDF-SDC FFT using Modified Carry Select Adder

In this paper, the pipelined Radix-2 SDF-SDC FFT using modified Carry Select Adder has been proposed. In the existing method of FFT, the power consumption is large and also the processing speed is low. The proposed architecture of pipelined 16 point SDF-SDC FFT using Modified CSLA has been illustrated in [Fig. 6].

The pipelined SDF-SDC FFT using carry select adder has been designed, that is used to reduce the power consumption but increasing the hardware slices .So, we modified the carry select adder circuit, which is to reduce the hardware slices, LUTs, delay and also power consumption. In the modified carry select adder, the full adder circuit is reduced. In the full adder circuit, the number of logic gates is reduced. Finally, the modified carry select adder circuit is integrated into Radix-2 SDF-SDC FFT processor. The main goal of this paper is to improve the processing speed and performances of the FFT processor.

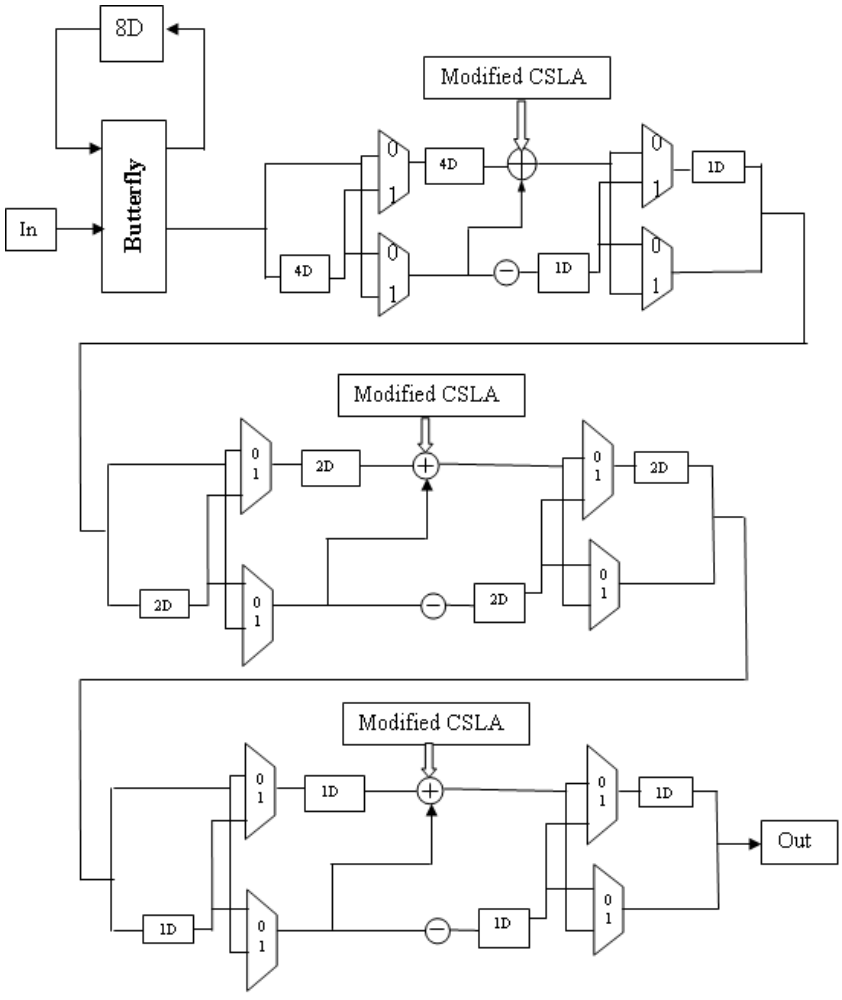

Fig. 6: Proposed architecture of pipelined 16 point SDF-SDC FFT using Modified CSLA

RESULTS

The proposed design of pipelined Radix-2 SDF-SDC FFT using Modified CSLA has been made by using Verilog Hardware Description Language (Verilog HDL). The simulation results has been evaluated by using ModelSim 6.3c and Synthesis Performances are estimated by using Xilinx 10.1i (Package: pq208, Family: Spartan-3, Device: Xc3s200) design tool. The simulation result of proposed pipelined Radix-2 SDF-SDC FFT using Modified CSLA is illustrated in [Fig.7].

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The performance evaluation of existing Radix-2 SDF-SDC FFT using carry select adder and proposed Radix-2 SDF-SDC FFT using modified carry select adder are analyzed and compared in Table 1. Also the performance evaluations are graphically illustrated in [Fig. 8].

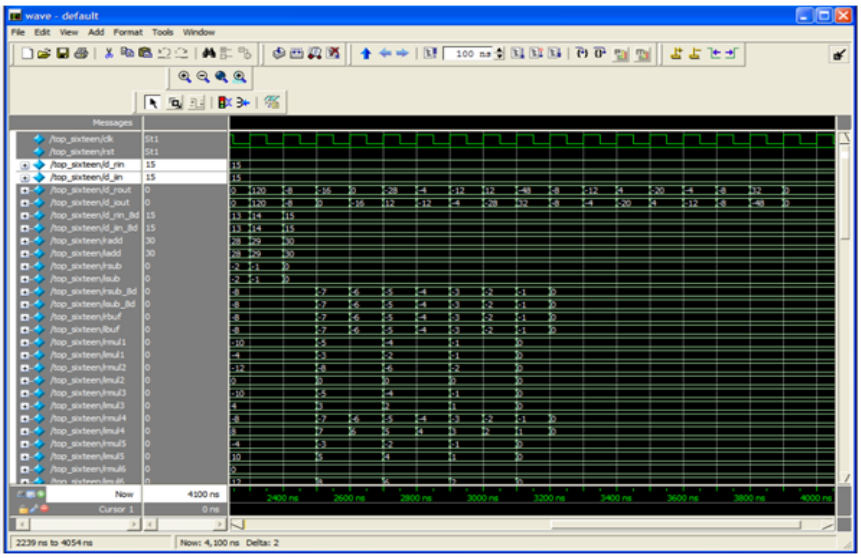

Fig. 7: Proposed pipelined Radix-2 SDF-SDC FFT using Modified CSLA

Table 1: Comparison of existing Radix-2 SDF-SDC FFT using carry select adder and proposed Radix-2 SDF-SDC FFT using modified carry select adder

Types/VLSI Concerns	Number of Occupied Slices	Total Number of LUTs	Delay (ns)	Power(W)
Existing Radix-2 SDF-SDC FFT using carry select adder	984	1714	43.760	3.778
Proposed Radix-2 SDF-SDC FFT using modified carry select adder	945	1679	41.456	1.370
Percentage Reduction	3.96%	2.04%	5.26%	63.7%

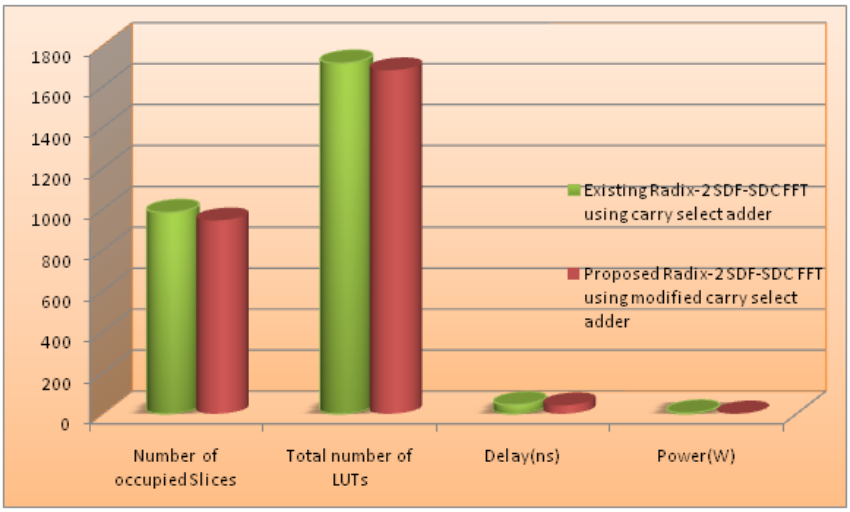

Fig. 8: Performance evaluation of existing Radix-2 SDF-SDC FFT using carry select adder and proposed Radix-2 SDF-SDC FFT using modified carry select adder

ISSN: 0976-3104

From [Table 1], it is clear that proposed pipelined Radix-2 SDF-SDC FFT offers 3.96% reduction in hardware slices, 2.04% reduction in number of LUTs, 5.26% reduction in delay and 63.79% reduction in power consumption than the existing Radix-2 SDF-SDC FFT. When compared to existing method, the numbers of occupied slices are 984 which is reduced to 945, the total number of LUTs are 1714 which is reduced to 1679, the delay value is 43.760ns which is reduced to 41.456ns, the power value is 3.778w which is reduced to 1.370w, than the proposed method. When compared to existing method, the proposed method gives better performance of the FFT processor.

CONCLUSION

Pipelined Radix-2 Single path Delay Feedback (SDF) – Single path Delay Commutator (SDC) FFT using Modified Carry Select Adder has been proposed through Very Large Scale Integration (VLSI) System design environment. Reduced full adder is designed using less number of gates compared to conventional Full adder. These reduced adders are applied in the carry select adder to analyze and improve the performance. The modified carry select adder is incorporated into Radix-2 SDF-SDC FFT processor. The main goal of this paper is to reduce the processing time and improve the speed of the FFT processor. The proposed method is used to reduce the slices, LUTs, delay and power consumption. The proposed pipelined Radix-2 SDF-SDC FFT offers 3.96% reduction in hardware slices, 2.04% reduction in number of LUTs, and 5.26% reduction in delay and 63.79% reduction in power consumption than the existing Radix-2 SDF-SDC FFT. In future, the proposed architecture will be absolutely useful in OFDM based digital communication to perform the function of frequency transformation and to analyze the spectrum characteristics of digital inputs.

CONFLICT OF INTEREST
There is no conflict of interest.

ACKNOWLEDGEMENTS
None

FINANCIAL DISCLOSURE
None.

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