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ARTICLE

NOVEL 2-BIT FULL ADDER DESIGN IN QUANTUM DOT CELLULAR AUTOMATA TECHNIQUE

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ABSTRACT

Back ground: *Quantum dot Cellular Automata (QCA) consists of a cell which includes two electrons logically interacting in the four quantum dot cell. QCA helps the design for faster speed, smaller size, and low power consumption.QCA is the new form of nanotechnology for many electronic circuits in VLSI paradigm.* ***Methods:*** *In this manuscript, QCA Designer 2.0.3 tool has been utilized for verifying the output of the circuit.* ***Results:*** *In this paper, the designs of 1-bit and 2-bit full adder are proposed which reduce the total number of QCA gates and its particular area and power consumption compared to previous well known designs.* ***Conclusions:*** *The proposed QCA full adder circuit saves up to 50% Cell counts and 67% Area composed to the previously reported designs.*

KEY WORDS
QCA, Inverter, Crossover Gate, Majority Gate, Full Adder

INTRODUCTION

QCA is a technology which stands for Quantum Dot and Cellular Automata. QCA is an advanced version in VLSI arena to implement IC designing than CMOS (Complementary Metal Oxide Semiconductor). CMOS was measured on micro-scale that was consisting of high density and had low power Very Large Scale Integration (VLSI) circuit [1-4]. The drawbacks of CMOS technology have high leakage current, power dissipation and limitation of speed in GHz range. Therefore, CMOS technology has been overtaken by QCA technology. In digital logics, adders are basic circuits. Adder circuits in conventional transistors required many wires; therefore the earlier adder circuit's speed was much less because of so many wires. Hence such circuit'simplementations were difficult. A Quantum dot Cellular Automata is used as a software program. Hence, in this software, the design of QCA has been implemented.

This paper consists of: Basics of QCA, proposed designs of 1-bit and 2-bit Full Adder, simulation result, discussion and conclusion.

MATERIALS AND METHODS

QCA design consists of some basic key points.

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QCA cell consisting of four dots

In QCA cell, it consists of quantum dots that are basically four dots in one square. From these four dots, only two dots are having electrons which are arranged diagonally to each other. The two electrons are not able to leave a cell; else they will be able to tunnel in between the dots as shown in [Fig. 1][5-8].

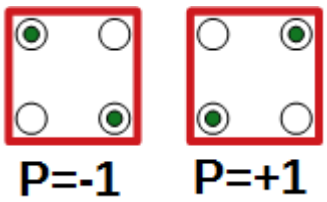

Fig. 1: Four dots of QCA cell.

Only two electrons are allowed to place in a cell, if two or more electrons are present in a cell, then Coulomb repulsion will come in contact and repulsion will take place. Hence, there are two polarization states that are P=-1 for logic 0 and P=+1 for logic 1.

Components of QCA

In a QCA inverter gate, the input is shown as A and output as A' which is shown in [Fig. 2]. To make the input A strong, same types of two cells are connected with each other and at 45 degree angle, the next cel is placed, which gives the output. Therefore, when A has the logic as logic 0 the output A' gives the logic as 1 and vice-versa.

3 input QCA majority gate is depicted in [Fig. 2]. A, B, C are given as the 3 inputs [9-11]. Suppose the input for A islogic 0 and input for B is logic 0then C is considered as AND or OR gate respectively depending on

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the polarization of either logic 0 or logic 1. The output is obtained from majority input from all the 3 inputs. If all the majority inputs are given as logic 0, so the output will become logic 0.

Wire of QCA cell-The wire of QCA cell can have the same polarization up to 10 cells for logic 0 or 1; after that logic will be different that is either logic 0 or 1. As the cells are connected to each other, therefore the long interconnection of wires is not needed.

Crossover Gate- When two QCA wires come in contact and if they don't form a majority gate [12-14]. The crossover gate is represented by clock 1 as horizontal wire and clock 3 as vertical wire. In any crossover gate there are two combinations of clocks, clock 0 with clock 2 and clock 1 with clock 3.

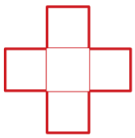
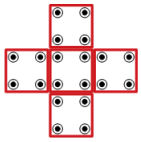
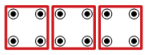
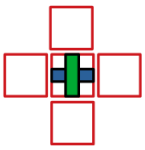
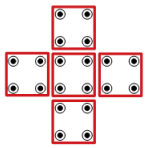
QCA Component	Symbol	Actual Symbol
QCA Inverter Gate		
3 Input QCA Majority Gate		
Wire of QCA cell		
Crossover Gate		

Fig. 2: Components of QCA symbols.

QCA clocks

In QCA clocks, it basically gives the direction of cells to control the flow of data. QCA includes four clocks: Switch , hold, release and relax. So the cells are given the direction of flow as per the clocks as 0,1,2,3 as shown in [Fig. 3]. In clock 0 the phase is to start, in clock 1 it will hold the cells, then in 2 clock the cells will be released and finally in the last clock that is clock 3 the cells will be relax and again start from clock 0 [15-20].

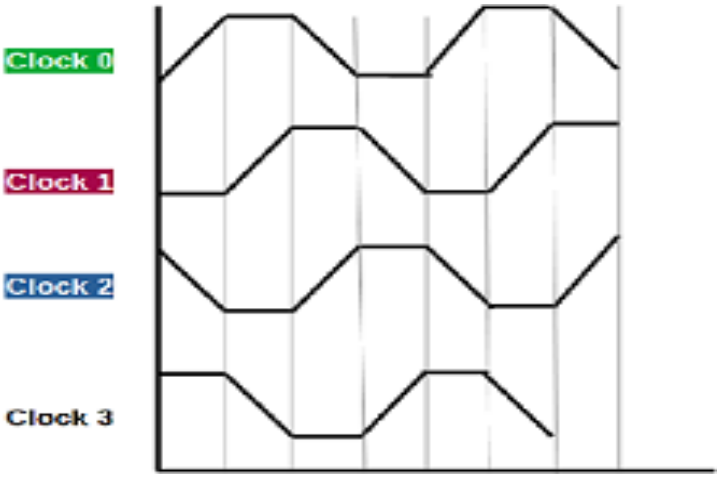


Fig. 3: Clocks in QCA.

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RESULTS AND DISCUSSION

Proposed design of 1-bit full adder

In the full adder circuit, there are three inputs namely A, B, Cin and output as Sum(S) and Carry (Cout).The truth table of 1-bit Full Adder is given in [Table 1].

Table 1: Truth table of 1-bit full adder

A	B	Cin	Sum (S)	Carry (Cout)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The equation of Sum(S) and Carry (Cout) is given as:

Sum = A'BCin' + A'B'Cin + AB'Cin' + ABCin

Cout= AB +BCin +CinA

Simulation result of 1-bit full adder

A, B, Cin are the inputs, Sum and Carry are the outputs for the given 1-bit full adder design as shown in [Fig. 4].

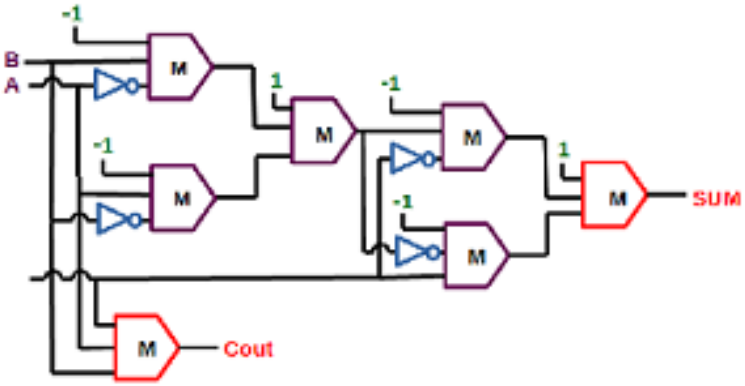

Fig. 4: Block diagram of 1-bit full adder using QCA gates.

In the 1-bit full adder design implementation as shown in [Fig. 5], the clocks are used depending upon the gates. The majority gate uses a separate clock cycle. If for AND operation Clock 1 is used then the same clock might be used for other AND operation also. If OR operation is used then Clock 3 is used to get the final output.

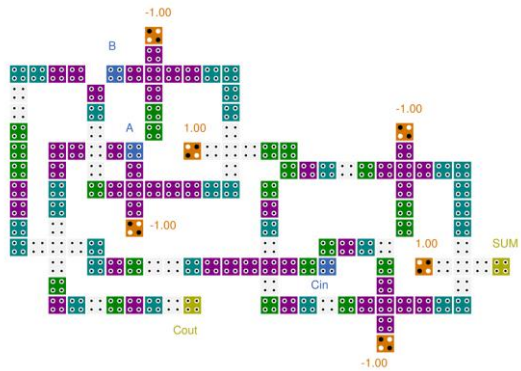

Fig. 5: Implementation of 1-bit full adder using QCA designer 2.0.3.

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Fig. 6 shows the simulation of 1-bit full adder having Sum and Carry (Cout) as an output.

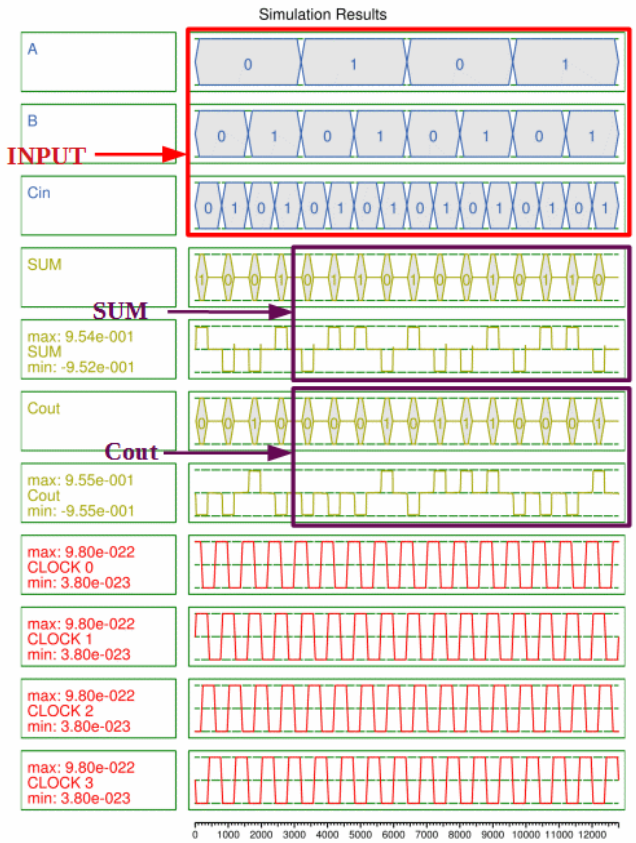

Fig. 6: Simulation of 1-bit full adder using QCA designer 2.0.3.

Proposed design of 2-bit full adder

The 2-bit Full adder comprises of five inputs namelyA0,B0,A1,B1,Cin and three outputs namely S0,S1,Cout. The truth table for 2-bit Full Adder is given in [Table 2].

Table 2: Truth table of 2-bit full adder

A0	A1	B0	B1	Cin	S0	S1	Cout
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	1	0	0
0	0	1	1	0	1	1	0
0	1	0	0	0	0	1	0
0	1	0	1	1	1	1	0
0	1	1	0	0	1	1	0
0	1	1	1	1	0	1	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0
1	0	1	0	0	0	0	1
1	0	1	1	0	0	1	1
1	1	0	0	0	1	1	0
1	1	0	1	1	0	1	1
1	1	1	0	0	0	1	1
1	1	1	1	1	1	1	1

Simulation result of 2-bit full adder

A0, B0, A1, B1, Cin are the inputs and S0, S1, Cout are theoutputs for the proposed 2-bit full adder design as shown in [Fig. 7].

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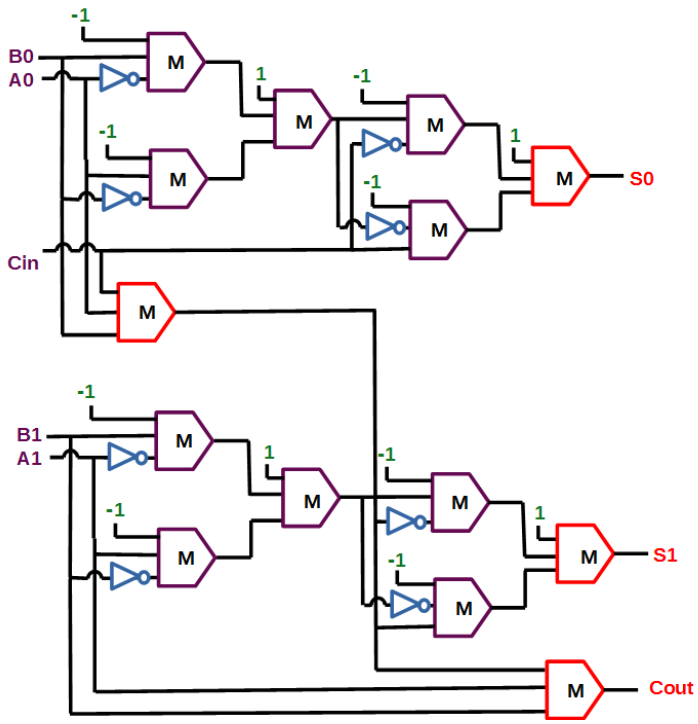

Fig. 7: Block diagram of 2-bit full adder using QCA gates.

In [Fig. 8], the implementation of 2-bit full adder design is shown.

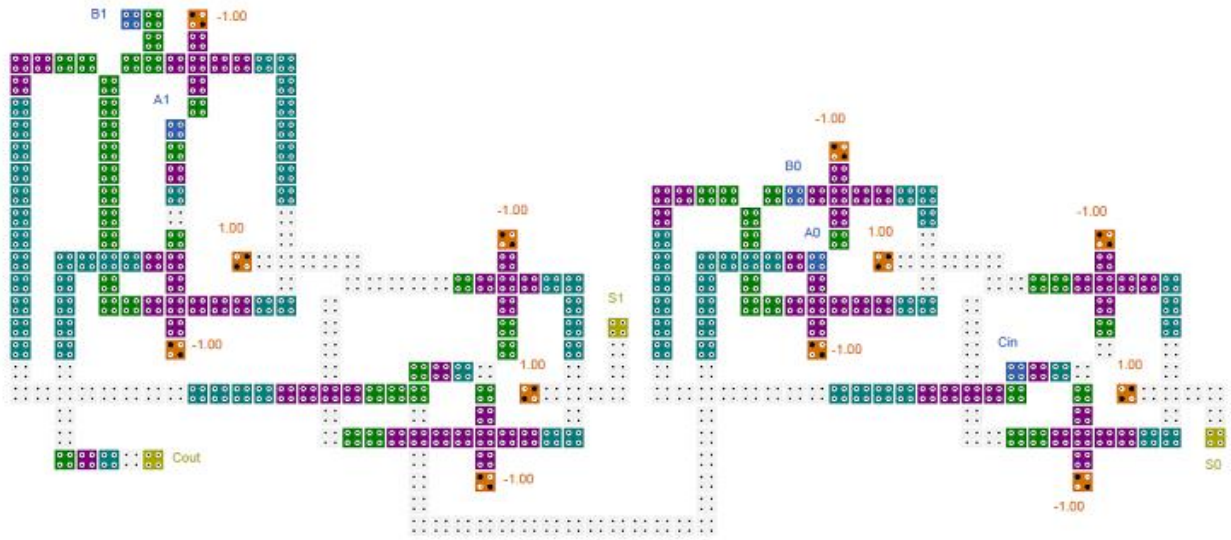

Fig. 8: Implementation of 2-bit full adder using QCA designer 2.0.3.

The simulation of 2-bit full adder is shown in [Fig. 9], which has Sum and Carry (Cout) as the output.

The proposed 2-bit full adder design saves up to 65 % of area and up to 50 % of total cell counts compared to the most recent available full adder design, shown in [Table 3].

The proposed mechanism and style of designing a Full Adder (FA) circuits are novel. The proposed FA uses crossover approach in its design which is best suited for designing any new circuit in QCA technology with minimum number of cells and area. Crossover approach gives a freedom to design the circuit in single layer only compared to multilayer approach, which requires more number of cells, latency and area. The proposed FA circuits are robust and accurate in acquiring its output.

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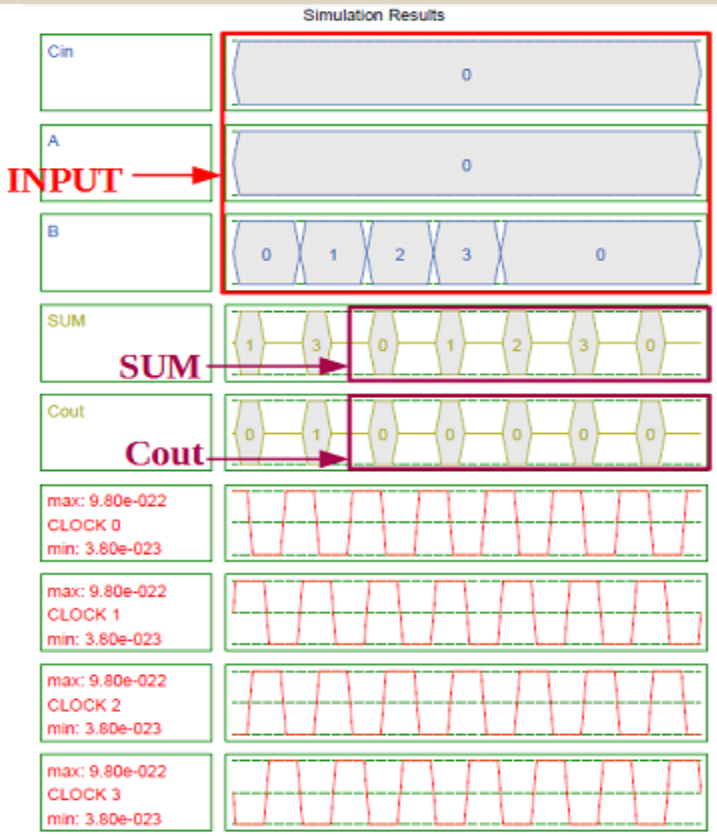

Fig. 9: Simulation of 2-bit full adder using QCA designer 2.0.3.

CONCLUSION

In these paper basics of QCA, wire of QCA cells, types of gates and QCA clocks have been discussed. The paper comprises of single layer input design on 1-bit full adder as shown in [Fig. 5] and 2-bit full adderas shown in [Fig. 8]. Full adder is a basic circuit in ALU and Microprocessor circuits, which needs to be design very carefully. The proposed 2-bit Full adder design uses 314 numbers of QCA cells, 2 clock latency and area of 0.53 μm^2. In the proposed 2-bit Full adder, the total number of QCA cells is45% less with almost 33% less area, compared to the previous latest designs. Therefore, the proposed QCA design circuits have fast speed, small size and power consumption is less. The proposed FA designs have the potential to be a basic reference designs for larger designs at digital VLSI technology.

CONFLICT OF INTEREST

There is no conflict of interest.

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FINANCIAL DISCLOSURE

None

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