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ARTICLE

AN MMIC LOW-NOISE AMPLIFIER DESIGN TECHNIQUE

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ABSTRACT

Low Noise Amplifier (LNA) is one of the most important components for today's communication systems. Lot of millimeter- wave application devices such as receivers; Trans receivers can't be imagined without LNA nowadays. As, it is necessary to suppress the noise interference within the signal for efficient communication and amplifiers are always used for enhancing the strength of the signal in order to cover the long distance communication. Therefore the use of LNA is highly necessary to improve the quality of communication. This paper made a brief attempt to present the design discussion of LAN's and its usability along with the application areas. The various technologies used for the manufacture of LNA and its progressive aspects are also discussed. Some major findings are also highlighted in the same area such as CMOS Broadband Low-Noise Mixer with Noise Cancellation, Noise Adaptive Channel Smoothing of Low-Dose Images

KEY WORDS
LNA, Two finger technique, On-wafer technique, MMIC technique, packaged amplifier

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INTRODUCTION

Increasing Low noise amplifiers are important components in mm-wave application such as radio astronomy, receivers for communication system, earth science radiometry, passive remote sensing and transceivers for radar instruments [1]. The invention of Inp HEMT, metamorphic HEMT, and InP HBT devices have enabled amplifiers to operate at exceptionally high frequency. Cryogenically cooling of HEMT amplifiers effectively reduce the noise level in very large amount [2]. Along with it is also used to improve the sensitivity of radiometers of astrophysics and earth observation instruments. Recently cryogenic result of 35-nm InP HEMT monolithic microwave integrated circuit have led to record noise above 100GHz [3]. Although the continuous research on this technology offer to design amplifiers at highest frequencies and with minimum noise temperature. There are several challenges faced by designers in the pathway; such as lower breakdown voltage and maximum high frequency of oscillation of the transistors. Due to these issues, a stable amplifier to fulfill the linearity of a wideband receiver, which requires high gain from LNA system, is very difficult to design [4]. The aim of this paper is to examine and finding the solution in order to take full advantage of the available latest technology.

The first design of three stages LNA is implemented at Northrop Grumman Corporation's, (country name and year). This design is implemented using 35-nm InP MMIC technology on InAs composite channel (IACC) HEMTs, which produced 23-K noise temperature at 108 GHz, when cooled cryogenically at 27 K[5]. This manufacturing process follows a fixed design procedure of MMIC LNA, where an appropriate gate width for the device is achieved by placing number of fingers in parallel manner within a single transistor to produce the lowest level of noise above 100 GHz along with possessing wide bandwidth and better linearity. While, designing wide band cryogenic LNAs, the design approach have some limitations especially regarding the stability of the amplifier. Therefore, a new parallel two-finger unit transistor MMIC LNA design technique is introduced [6], which enables the design of wideband, high linearity, and first-time-right LNAs with very stable, predictable, and repeatable operation at cryogenic temperatures.

The first design cycle amplifier based on this design approach achieve more than 20 dB gain over the range of 75 GHz to 116 GHz frequencies and produced 26 to 33 K noise temperature with high stability as compare to the conventional amplifier. Later, a new method is proposed to predict the stability of a multi-finger transistor using two-finger transistor model [7]. This method also verified the hypothesis i.e. "odd-mode or loop oscillations can occur within a multi-finger transistor is due to the asymmetry of the transistor [8].

The paper presented here, is organized as follows. At first, fundamentals of selecting a proper device size for a LNA is discussed and followed by the design of a conventional multi-finger HEMT amplifier. After that the MMIC LNA design technique is introduced followed by On-wafer and package amplifier design approach

THE SELECTION OF AN APPROPRIATE SIZE FOR THE DEVICE

The selection of the appropriate size transistor is the most crucial part of the amplifier designing. For keeping the miniature size, at first select an optimized width of gate and design a single finger. Now with the help of these fingers, the full transistor is designed [9]. The gain and the noise parameters of the transistor designed through this technique are not affected significantly by the number of fingers. These numbers are only responsible for producing a small change which is due to the distributed effects of connecting wires [10]. These numbers are contributing their effects in device impedance and power capability. While designing the High Electron Mobility Transistor, this technique plays an important role to optimize it. As the HEMT is start operating from very high frequency (approximately 2 GHz) and at this high

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level of frequency there is huge chances of generating high noise [11]. Therefore it is challenging task for the researcher to design HEMT with low sound temperature along with lower break down voltages. In this technique, the gate is designed with very low resistance, which contributes its effect to reduce the noise. It also helps to enhance the gain value of the transistor [12].

STUDY OF MULTI-FINGER HEMT INSTABILLITIES

Two finger transistors are symmetrical in architecture. In this transistor, drain is in the middle position and the sources are present at both side of the drain. However, the HEMT transistor more than two fingers also having the sandwich structure with drain and sources, keeping drain in the middle but here the drains and sources are connected. Due to these internal connections, the parasitic impedance of the HEMT structure increases, which deviates it from the ideal structure, which makes the cryogenic modeling of this transistor is very important. Apart from this to predict the stability of this transistor is also very challenging due to its higher frequency up to 1 THz. Again the transconductance and the frequency value rises considerably higher at cryogenic temperatures, which again influence the stability factor of this transistor [8]. Again, due to the asymmetry present in its structure, the phenomenon of loop oscillation is developed, which again decorate its stability at high frequencies. This developed loop oscillation affects the drain current and enhance it drastically. Due to this jump in drain current, the net gain of this transistor decreases and the noise temperature increases up to the 10-20 K. To cope up with these instabilities arises in four finger transistor, the model is suggested, which developed the targeted amplifier using two finger transistors only. According to this model, at first the four finger transistor is developed using two finger transistor and the air-bridges present in the structure are modeled using inductors having value 10 pH. The amplifier made up using this model, having showing better performance as compared to the previous one [11].

NEW PARALLEL TWO FINGER TRANSISTOR LNA DESIGN TECHNIQUE

This technique is also focuses towards the instability issues arises in the multi-finger transistor. This method is proposed by Yang in 2013 [13]. According to this model, at first a two finger transistor is optimized for the desired frequency using T_{casmin} technique. The impedance is designed through the number of unit cells and these cells also control the output power. Once the numbers of unit cells are selected according to the requirement of the application, it is fed in parallel wise manner with the help of matching networks and power division sections [14]. Now using these two finger transistors, multi-finger transistor are constructed. Due to use of unit cells for designing, the scalability of the multi-finger transistor increases. It also helps to reduce the complicacy of routing network. In this way, this model avoids the stability issues of multi-finger transistor and also provides better control over the linearity of the amplifier [15]. Though, due to the presence of matching and power division network, this model having higher losses at the input side.

DESIGN OF AN LNA USING THE PARALLEL TWO-FINGER UNIT TRANSISTOR

In various designing techniques, it is observed that the utilization of a multi finger transistor produced oscillations that occur within the transistor [16]. As to overcome from this stability issue, this method dedicated to divide the four finger transistor into two finger transistors with same input and output conditions. For designing this, at first the low-impedance transmission line is used in series wise manner for matching the input and output. This transmission line is also used for power dividing and combining purpose. If this layout is not properly designed then three different types of oscillation will initiated named as even mode oscillation, odd mode oscillation and hypothesized mode oscillation. The even mode oscillation is similar as the oscillation produced in conventional amplifier using four finger devices [17]. The odd mode oscillations occur due to the on chip dividing and combining process. The hypothesized mode oscillation problem occurs within the single finger transistor. Hence, this method is simpler in design and produces circuit with enhance stability along with excellent performance [18].

MMIC Amplifier Technology

MMIC stands for monolithic microwave integrated circuit. The word monolithic is derived from the Greek letter "Monos (single)" and "Lithios (stone)". Thus, these circuits are built on a single crystal. MMIC amplifiers are a type of integrated circuit device that operates at microwave frequencies (300 MHz to 300 GHz). This device typically performs function such as microwave mixing, power amplification, low noise amplification and high frequency switching [19]. It posses high dielectric constant (9 or higher) and low dissipation factor or loss tangent. The permittivity of MMICs should be remains constant over the entire temperature range of interest. The major features of MMICs are having high purity, constant thickness, high surface smoothness, high resistivity, high thermal conductivity and dielectric strength, which make them easier to use as cascading. Again it does not require any external matching network, while cascading. MMIC are generally fabricated using Gallium Arsenide and A III-V compound semiconductors [20]. The metal oxide semiconductor field effect transistors (MOSFETs) are used as the active device in MMIC amplifier. However, recently high electron mobility transistors (HEMTs), pseudomorphic HEMTs and heterojunction bipolar transistors become more prominent replacement as the active device in MMIC amplifier. The [Table 1], shown below highlights some previous work done on MMIC amplifier technology.

Table 1: Notable Previous work on MMIC Amplifier Technology

S.no	Author	Objective	Advantages	Limitations	Reference
1.	Bo Chen et. al.	To design a broadband MMIC low noise amplifier	1. A 2dB noise figure from 25 GHz to 40 GHz is achieved. 2. Less noise figure is obtained	1. Signal gain is small 2. Sensitive to the resistance of matching network.	[21]
2.	Dongsu Kim et. al.	To develop a Compact and Low-profile GaN Power Amplifier Using Interposer-based MMIC Technology.	1. Capable to integrate heterogeneous IC's 2. Compatible with various microwave and millimetre-wave systems. 3. Having high degree of design flexibility. 4. Low cost.	1. It can't be realised using a single MMIC technology.	[22]
3.	YounSub Noh et. al.	For using Ka-band GaN Power Amplifier MMIC Chipset for Satellite and 5G Cellular Communications	1. Increased in gain. 2. Increased in efficiency. 3. Compact in size.	1. Having return loss at same frequency. 2. 2. Complex design.	[23]
4.	K. Tsukashima et. al.	To develop transceiver MMIC's for Street Surveillance Radar	1. Miniature chip size. 2. It can be directly flip-chip on assembled board.	1. Performance is varied with temperature. 2. Complex design	[24]
5.	Amin Ezzeddine et. al.	To develop broadband MMIC Power Amplifier for multiple wireless systems	1. Low cost production. 2. It has good linearity and high power density 3. 3. Achieved good efficiency and o/p power.	1. High ohmic loss.	[25]
6	W. Simburger et. al.	To develop 1.3W 1.9GHz and 1W 2.4GHz power amplifier MMIC in silicon	1. It is very low cost power amplifier. 2. High output power 3. Good input impedance matching 4. Power efficiency is high	1. Large amount of current are loss.	[26]
7	Shigeo KAWASAKI et. al.	To develop a High-gain and Low-Noise MMI Amplifier Module for Ku-Band antenna.	1. Low noise 2. Compact in sized 2. 3. Cost is low	1. Return loss is high	[27]
8	Diana Zhang et. al.	To develop a Novel GaAs Multi-Chip MMIC Video Amplifier for Optical Receiver in cable Communication systems	1. Receiver gain is high. 2. Having wide optical dynamic range. 3. High sensitivity and linearity. 4. Low power consumption.	1. High RF output over weak input optical signal. 2. Having high input impedance. 3. Uses very expensive coaxial cables.	[28]
9	A. Leuther et. al.	To develop 50nm sized MMIC amplifier for 480GHz	1. Cost effective 2. Highly robust and process yield 3. Compact design	1. Working at low frequency only	[29]
10	Yeoung chang chou et. al.	To manufacture a reliable 0.1um AlSb/InAs HEMT MMIC Technology for ultra low power application	1. Consume less power 2. Reduced noise 3. High speed 4. High performance	1. Costly	[30]

On-Wafer Measurement

Nowadays, microwave wafer probing measurement technique is accepted and applied worldwide as one of the efficient techniques in microwave IC development. The major attraction of this method is its resolution and

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repeatability of calibrations which is possible at the probe tips along with it is very convenient and having high throughput [31]. This *measurement method is used to determine* S-parameter of On Wafer active devices in between from 500MHz to 40 GHz [32]. This measurement technique required some fixed fixtures (electrical as well as mechanical) such as wide bandwidth transmission, low contact of resistance, consistent probe shape, placement of probe, durability etc. Microwave probe transmission line contact precisely with the impedance right to the ground-signal-ground-contact. For the measurement procedure, at first turn on the equipment approximately one or two hours before calibration has done. Take care that the probe, which is mounted at 150um and set all dc voltage to zero, ensures that the probes are in place. The cables need to be clean and tight and the torque will be using relevant wrench IPA along with the clean and dry connectors. The probe tips are inspected and clean if it is contaminated. The positioner planarity is adjusted until all tips make even contact with the substrate. Now, set the basic parameters for the measurement such as frequency range, power level, type of sweep etc. and get the required data of measurement. The table given below [Table 2] represents the advantages and limitations of some previous works on On-Wafer measurement technique.

Table 2: Notable Previous work on On-Wafer Measurement Technique

S.no	Author	Objective	Advantage	Limitations	Reference
1.	G. Dambrine et. al.	To measure on-wafer high frequency noise of FET's	1) Automatic tuner is not required 2) Easy to develop on conventional microwave probe wafer system 3) The modification of input admittance is performed near the device.	1) Required calculations are complicated.	[33]
2.	Chen Liu et. al.	on-wafer measurements using 10-term error model	1) Better than conventional SLOT method. 2) Improved measurement accuracy.	1) Probe coupling should be corrected. 2) More difficult to characterize.	[34]
3.	Ryo Sakamaki et. al.	To improve the on-wafer measurement accuracy at millimetre-wave frequencies	1) Improvement in verification process. 2) A precise s-parameter measurement is realised	1) Probe positional variation is limited by optical wavelength. 2) Required more skilled person for measurement	[35]
4.	Aihua Wu et. al.	To develop a Verification Technique for On-wafer Noise Figure Measurement Systems	1) The measured NFs have a good agreement with the references for both the 1 dB and 3 dB attenuators as-long-as the effect of bondwire is removed.	1) The cascaded network consists of a mismatched attenuator and a LNA. 2) The measured NFs are not related to the injected noise signal but strongly dependent on source match. 3) Not capable to verify the noise measurement system.	[36]
5.	Luuk F. Tiemeijer et. al.	To characterize On-Wafer Noise-Figure	1) Able to measure the differential noise figure 2) Not affected by the common mode port terminations.	1) At 60 GHz, the path difference between the balun and device- under-test (DUT) must be less than 70 m, to keep the phase error below 5^0.	[37]
6.	Inder Bahl et. al.	Automatic Testing of MMIC Wafer	1) Achieved good accuracy at maximum operating frequency. 2) Achieved good dimension.	1) Calibration is highly required by skilled person 2) Unit and Probe change/degradation will highly affect the results	[38]
7.	Takuya Imamoto et. al.	To reduce the low-frequency noise in	1) Off-leakage current is reduced	1) The performance of	[39]

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		vertical MOSFETs	2) Consume less time 3) Low cost	the circuit is decreases due to the elimination of back bias	
8.	Christopher T. Coen et. al.	To design and characterized G-Band SiGe HBT Low-Noise Amplifiers	1) Improved gain performance.	1) High noise 2) Integration capabilities are low	[40]
9.	Troels Emil Kolding et. Al.	To establish a new method (Four-Step Method) for De-Embedding Gigahertz On-Wafer CMOS Measurements	1) The extraction method is very strong. 2) It accurately predicts the series losses.	1) Higher numerical complexity than conventional CBD method. 2) Not fully comfortable with specified layout guidelines.	[41]
10.	David E. Bockelman et. al.	To measure the Mixed-Mode S-Parameters of Differential Circuits using Pure-Mode Network Analyzer	1) More accurate 2) Less numerically complex 3) It has ability to generate simulated mixed-mode - parameters from CAD.	1) Difficult to make pure mode system. 2) Having residual errors in calibration. 3) Metal and dielectric losses are present	[42]

Packaged Amplifier Technology

Packaged amplifier is strongly depends upon the operating frequency. In this amplifier to achieve the high accuracy and maximum power transmission, a matching network is required on the input and output to minimize the reflection problems [5,10]. It is of very low cost and compact in size. The major advantage of packaged amplifier is its ability to work on both (AC and DC) power supply and gives high performance over the wide frequency range. Again, it includes current limiter circuit for failure protection purpose due to the over heat [6]. The [Table 3], shown below highlights some previous work done on Packaged amplifier technology.

Table 3: Notable Previous work on Packaged Amplifier Technique

S.no	Author	Objective	Advantage	Limitations	Reference
1.	Abdul R Qureshi et. al.	To develop the more efficient RF power amplifiers	1. Energy efficiency is high. 2. The power combining networks is simple and compact. 3. Having high data rate for mobile communication	1. Cost is high 3. Having more complex modulation system	[43]
2.	Maciej Myslinski et. al.	To establish a large signal Behavioral Model for Packaged RF Amplifier		1. Very high cost. 2. Heavy weight. 3. Having higher harmonics	[44]
3.	Gary (Guohao) Zhang et. al.	To develop a linear amplifier architecture and its packaging technologies for new generation smart phone applications.	1. Low cost. 2. Compact in size and good performance 3. Having high efficiency at low power. 4. Good thermal dissipation.	1. Load sensitivity is low.	[45]
4.	Kris kong et. al.	To develop a compact 30 GHz MMIC High Power Amplifier	1. Output power performance is high.	1. Expansive product 2. Having small signal response.	[46]
5.	Jiajie Tanga,b, Huajiang Wanga,b et. al.	An MCM Package Process for 24GHz Driver Amplifier Using Photosensitive BCB	1. Higher density. 2. better performance 3. higher reliability 4. low cost 5. MCM is one of the important steps of 3-dimentional High Density Packaging.	1. The interlayer-connection resistance is 75mΩ which is not as good as that of the MCM manufactured with dry-etch BCB.	[47]
6.	Plextek RF I	To develop 5W X-	1)GaN(Galium	1) It produces high	[48]

		Band GaN Power amplifier using discrete plastic packaged SMT transistor	Nitride) discrete transistor is readily available. 2) Low cost. 3) Easy to handle. 4) High stability at frequency above 12.5GHZ.	thermal noise. 2) Efficiency is low.	
7.	Jong-Min Lee et. al.	To develop wideband transimpedence amplifier	1)Wideband transimpedence amplifier 2) Quality of voltage signal is high. 3) Performance is good	1)Highly complex circuit design. 2) Power loss due to high transimpedence	[49]
8.	Dusan N. Gurjic et. al.	To estimate the power amplifier package model using sweep measurement	1)it has very high frequency range operability 2)it has wideband frequency response 3) Power output is maximum	1) Expensive and complex 2) Difficult to construct	[50]
9.	Kris Kong et. al.	To develop a compact MMIC high power amplifier in chip for 30GHz	1)Low cost 2)High gain 3)Output power performance is high	1)Low impedance transmission 2) Condition specific	[51]
10.	Ravi Gugulothu, Sangam Bhalke et. al.	To characterized GaAs MMIC C-Band amplifier	1)Produces good gain and 2)Output power is high	1)Expensive 2)Condition specific	[52]

CONCLUSIONS

At present scenario, the multi-finger transistors are one of the necessary devices in order to perform several required applications, which are of human need and make our life easier. It was also verified that oscillations can occur with-in a multi-finger transistor and it works on high frequency that design to analyze frequency of that amplifier. These oscillations are not in favor of the stability of that transistor or making adverse effect on the stability of the entire amplifier. Therefore, it is highly necessary to prevent these effects. More precious, the technique is predicting for the stability of a multi-finger transistor using a two-finger transistor model is discussed. The oscillation is inferred by the using of dc measurements. These types of instabilities limit give the opportunity for choosing the appropriate device impedance and also the output power capacity of that transistor. Through overcome from stability problem of multi-finger transistors; design a parallel two-finger unit transistor MMIC LNA design technique that gives the full benefit of latest sub-50-nm HEMT technology. The design which is based on this design approach and it achieves better result comparable to the W-band cryogenic amplifiers. This shows that the new design approach is attractive for the design of LNA because it gives high gain and linearity which is very useful in design wide-band receiver system. Again it will be applied to reduce the noise figures and improve the gain. There is also work needed for the enhancing the bandwidth and linearity. Also the frequency application range is needed to be increase on and above 100 GHz in order to fulfill various application lie in a future need.

CONFLICT OF INTEREST
None

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