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DESIGN OF A NOVEL ARRAY MULTIPLIER USING ADIABATIC LOGIC IN 32NM CMOS TECHNOLOGY

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ABSTRACT

Aim: The paper presents a new adiabatic multiplier circuit based on Complementary Energy Path Adiabatic Logic(CEPAL). The proposed multiplier consumes lesser power when compared to the conventional CMOS multiplier. The proposed adiabatic array multiplier performs 8 bit multiplication. The proposed adiabatic multiplier is also designed with leakage reduction technique the performnance of which is better when compared to the CMOS multiplier. The operating speed of the complementary metal oxide semidonductor is increased. This paper presents the implementation of adiabatic CEPAL multiplier using CMOS. The measurement results of the adiabatic CMOS Multiplier demonstrates a reduction in power and reduction in energy. The operating frequency is in GHz range. These results shows that the propoed circuit can be used in high speed application. The proposed adiabatic circuits are designed in HSPICE using predictive technology models (PTM) in 32nm CMOS Technology. The experimental results for the proposed adiabatic designs demonstrate their effectiveness with energy consumption and with power optimization.

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KEY WORDS

CMOS, adiabatic logic, Adder, NAND gate, shorted gate, energy efficient, power optimization.

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INTRODUCTION

In recent times, mobile devices are emerging in faster rate replacing the existing devices which are bulky and consume more power. The mobile devices have high device density and is computationally faster. But increase in device density increases the power consumption. Circuits fabricated in CMOS technology below 65nm have less control over temperature and power wastage happens due to leakage current. Even though full swing voltage mode CMOS logic styles have been extremely successful they suffer from the lower limit of power dissipation on CLVdd2/2 during switching instants. So new methodologies and technologies are evolved to solve the problems occurring due to undesired power dissipation. Adiabatic circuits have power dissipation lower than the limit level of CMOS. But the speed of operation reduces. The total energy is reduced through energy recycling which is the basic concept behind adiabatic. Power supplies are pulse shaped and to be designed separately to meet the required load. In literature the adiabatic circuits are proved to have the best performance in power consumption. For computing units in processor core, faster and low power processing elements (PE) are required. Circuits like inverters, adders, multipliers, shifters and latch for the basic building blocks of a microprocessor or digital signal processor. Several adiabatic logics are proposed in literature like ECRL [1], differential logic [2], Dual rail [3], pass transistor [4] etc. In the literature chanda et al [5] proposed a multiplier architecture based on Urdhva Tiryakbhyam in CMOS adiabatic logic. A NxN vedic multiplier is designed using sum block, carry block and NAND-AND adiabatic block. For the implementation energy efficient adiabatic logic (EEAL) is used. The work is carried out in 180nm technology. The power can be further modified in this work by implementing in a 90nm technology or utilizing a different adiabatic logic instead of EEAL.

Cancio Monteiro et al [6] proposed a charge-sharing symmetric adiabatic logic (CSSAL) multiplier. The paper reports the NAND/NOR logic and their implementation in multiplier. The advantage of the proposed circuit is nodes internal to the circuit is maintained at same charge for the different combinations of input. The disadvantage is the less successful of the method at higher frequencies so used in cryptography applications.

In literature [7] a two phase clocked adiabatic static CMOS based Baugh wooley and Wallace tree multiplier is designed. The paper reports that the Wallace tree Multiplier shows less power consumption about 62.66%

compared to Baugh wooley multiplier. The implementation is done in 45nm which is troublesome when leakage current is considered.

Hardik Sangani et al [8] proposed a multiplier based on the classical ancient Indian vedic sutras. The structure of the multiplier is based on energy recovery logic. The operating frequency reported was 25MHz at 45nm which is lower. Similar work is done in the literature [9], a vedic multiplier implementation using CMOS, PFAL and ECRL. The work presents that the PFAL circuit provides better performance when compared to CMOS and ECRL. Still other multipliers were designed using Adiabatic XOR gates and sleep mode transistor logic [10]. A combination of sub threshold circuit and adiabatic logic design is utilized for the design of a multiplier. The circuit is driven by two power supply which is an AC signals with different amplitude and frequencies. The implementation is done in 180nm technology with skew tolerance circuit. A 4×4-bit Multiplier LSI Implementation of Two Phase Clocking Sub threshold Adiabatic Logic And adiabatic ultra low power multiplier is proposed in reference [11]. The reported frequency of operation is 1 kHz.

ADIABATIC CEPAL STRUCTURE

The limitations in irreversible ERL adiabatic logics like high switching activity caused by the most dynamic characteristics, need for multiphase and multiple-clock operations, design of a trapezoid or triangular PC(s), interlaced circuit configuration, differential signaling and output floating. The other problems occurring are oscillations of PCs through output tracking which causes power loss during adiabatic switching therefore occurs in every half of PCs cycle. Even in the QSERL circuit the throughput is closely related to the frequency ratio of the input to PCs and a valid logic at the input must occupy a whole PC cycle including the evaluation and hold phases otherwise the circuit may fail during evaluation. These problems leads to noise susceptance due to floating in output.

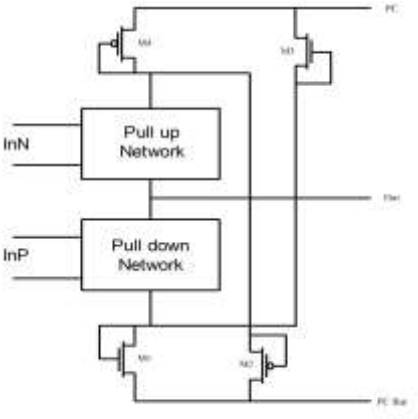

Fig: 1. Structure of a CEPAL logic

The CEPAL structure is given in **[Figure- 1]**, P1 and P2 are charging transistors and N1 and N2 are discharging transistors. With a pull-up and a pull-down Network the structure has two paths. For the initial operation assuming that the output is LOW, the pull up network is ON while the pull down network is OFF, the output follows either PC or its complement as it swings HIGH. This makes the power clock swinging down and the output node to become floating. But this situation is immediately removed when the power clock swings up. The CEPAL based AND gate is shown in **[Figure- 2].**

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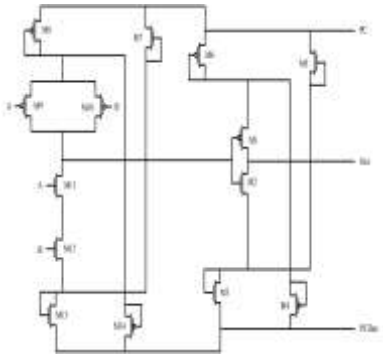

Fig: 2. CEPAL AND gate structure

Processing elements in DSP architectures

In DSP applications design of Filters is the critical block which deals with lot of computational units. The filter structure differs from application to algorithm specific. The adders, multipliers, shift registers, inverters, buffers are the different components of the filter structure. The multiplier is the most critical unit and requires an optimized structure based on partial product reduction, multioper and options etc. In multipliers the partial products are first generated and finally combined to obtain the final product. In this work the multiplier is optimized in the adder block where the number of transistors are reduced by 80% compared to the conventional adders. For partial product generators the array multiplier and vedic multiplier are implemented using adiabatic logics. The adder designed in this work is based on CEPAL adiabatic logic. As explained earlier, the adder design is a prime concern for the implementation of an efficient multiplier. The proposed adder is more suitable for efficient implementation of large operand adders. However, these designs are very efficient in terms of power consumption but special power clock generator circuits are required which is not the scope of this paper.

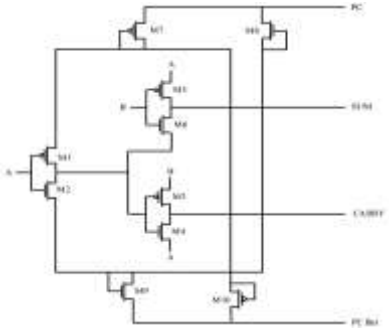

Fig: 3. CEPAL Adder structure

Multiplier

Easy to design and smaller in size features corresponds to the array multiplier. As the name indicates it uses parallelogram technique in its operation. The partial products are generated at the same time. The combining adder receives the partial products as inputs and produces the output. The multiplier is well suitable when performing the matrix multiplication. The structure is regular such that the vertical and horizontal delays are same. The critical path delays in the terms of full adder and gate have same value. Implementation of DSP algorithms with pipeling can be made easy using array multipliers. Array multiplier is shown in **[Figure- 4]**

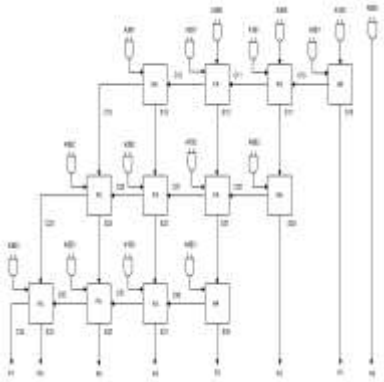

Fig: 4. Array multiplier using conventional adders

PROPOSED CMOS CEPAL MULTIPLIER

CMOS based adiabatic CEPAL processing element implementation using half adder, full adder and multiplier is proposed. The proposed array multiplier block diagram is shown in **[Figure- 5]**. The implementation of the proposed circuit for multilier is shown in **[Figure- 6]**.

The basic advantage of 6T half adders is smaller area and lower power utilization. It becomes more not easy and even obsolete to keep full output voltage swing operation as the design with fewer transistor count and lower power utilization are pursued. In pass transistor logic the output voltage swing may be degraded due to the threshold voltage defeat problem. The reduction in voltage swing leads to lower power consumption but may also lead to slow switching in the case of cascaded operation such as ripple carry adder. A low VDD operation the corrupted output may even cause break down of circuit. The smallest voltage that 10 T adder can work at 0.7V. The excessive power dissipation and long delay are attributed to the threshold voltage drop problem and the poor driving capability of some internal nodes at input combinations that create non full-swing transitions. The elimination of the path to the ground reduces the total power use by reducing the short circuit power. The combination of low power and low transistor add up makes the SERF adder circuit a viable option for low power design.

In this paper, we will propose a novel full adder design featuring complementary and level restoring carry logic (CLRCL).The goal is to reduce the circuit complexity and to achieve faster cascaded operation. The strategy is to avoid multiple threshold voltage losses in carry chain by proper level restoring. We first rewrite the full adder and Boolean functions as

$$\mathrm{Sum} = (A \oplus Cin) \cdot \overline{Cout} + (A \odot Cin) \cdot B$$
$$Cout = (A \oplus Cin) \cdot B + (A \odot Cin) \cdot A.$$

"Urdhva Tiryagbhym (UT)" sutra based multiplier. The multiplication algorithm based on the vedic sutra Urdhva Tiryagbhym is faster and consumes low power. The sutra performs vertically and crosswise operation between the different digits of the multiplier and multiplicand. The partial product and sum are calculated in a single iteration step. The vedic based multiplier is implemented to compare the performance of the proposed circuit.

Table: 1. Power and energy analysis of Half adder

Circuit	Power clock= 1GHZ				
	P_{avg} (W)	Iavg(A)	VDD(V)	(Tstop-Tstart)(s)	E(J)
Conventional	2.29E-05	1.45E-05	1	9.99E-07	1.45E-11
CEPAL conventional HA	1.23E-05	6.72E-06	1	9.99E-07	6.72E-12
CEPAL proposed HA	7.85E-05	5.81E-07	1	9.99E-07	5.80E-13

Table: 2. Power and energy analysis of Half adder

Circuit	Power clock= 1GHZ				
	P_{avg} (W)	Iavg (A)	VDD(V)	(Tstop-Tstart) (s)	E(J)
Conventional	8.12E-05	1.77E-05	1	9.99E-07	1.76E-11
CEPAL conventional FA	8.70E-05	2.49E-06	1	9.99E-07	2.48E-12
CEPAL proposed FA	7.93E-05	5.04E-07	1	9.99E-07	1.04E-13

Table: 3. Power and energy analysis of Half adder

Circuit	Power clock= 1GHZ				
	P_{avg} (W)	Iavg (A)	VDD (V)	(Tstop-Tstart) (s)	E(J)
CEPAL proposed 4X4 VEDIC MULTIPLIER	7.64E-04	3.04E-05	1	9.99E-07	3.04E-11
CEPAL proposed 4X4 ARRAY MULTIPLIER	6.44E-04	1.60E-05	1	9.99E-07	1.60E-11

For the implementation predictive technology model for 32nm is used. The supply voltage is 1V. The number of transistors is 14, 10 and 76 for full adder, half adder and multiplier respectively. XOR and AND gate having 14 transistors and 6 transistors respectively are used for the design of adder. The array structure for 8 bit results is shown. The circuit is faster in the operation and consumes lesser power and energy. The power and energy analysis for the conventional and proposed half adder is shown in **[Table- 1]**.

From **[Table- 2]** The results show that the power dissipation in conventional FA is more compared to the proposed. The proposed multiplier dominates and outperforms the vedic multiplier design. The vedic multiplier is faster when implemented in an non adiabatic way but still suffers from the number of transistors used. But when comes to adiabatic logic, the CMOS CEPAL based multiplier performance is better. **[Table- 3]** shows the comparison table for the two multipliers. The circuit runs with a power clock of 1 GHz. The power consumption is reduced by 15 % and energy consumption by 47%.

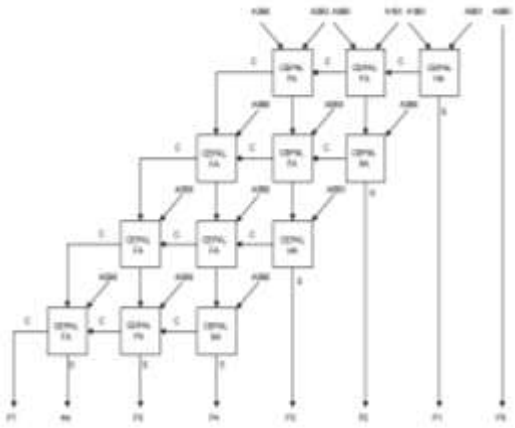

Fig: 5. Proposed Array multiplier using CEPAL adiabatic logic

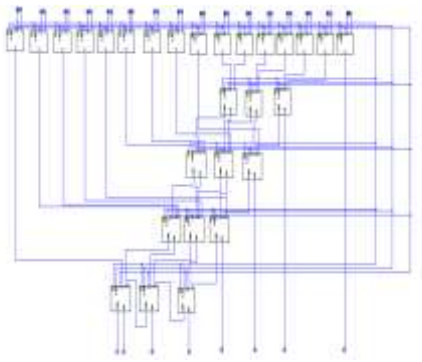

Fig: 6. Proposed Array multiplier implementation using CEPAL adiabatic logic

CONCLUSION

A new adiabatic multiplier circuit based on Complementary Energy Path Adiabatic Logic (CEPAL) is proposed in this paper. Compared to the conventional methods the proposed circuit is advantages. The proposed multiplier consumes less power and energy when compared to the conventional multiplier. The proposed adiabatic array multiplier performs 8 bit multiplication and is designed with leakage reduction technique. The measurement results of the half adder, full adder and adiabatic CMOS Multiplier demonstrates a reduction in power and reduction in energy. The power clock frequency is set to 1GHz. The implementation were carried out using HSPICE tool with predictive technology models (PTM) in 32nm CMOS Technology.

CONFLICT OF INTEREST

The authors declare no conflict of interests.

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None

FINANCIAL DISCLOSURE

None

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