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ARTICLE

AN AREA EFFICIENT FIRST ORDER POLYNOMIAL CONVOLUTION INTERPOLATION FOR VISUAL COMMUNICATION SYSTEMS

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ABSTRACT

Image interpolation is widely used in various visual communication systems like digital television broadcasting, digital cameras, tablets, mobile phones and display devices. A better quality of the image can be obtained by using image interpolation with higher order polynomials which require complex computations. In addition to high performance, an area efficient implementation is preferred for a variety of consumer applications. The first order polynomial convolution interpolation (FOPCI) is an algorithm in which the first order polynomial is used to reduce the complexity and to maintain the image quality. This work uses low area weighting coefficient generator for FOPCI. The proposed low complexity very large scale integration (VLSI) architecture is implemented on Virtex VI field programmable gate array (FPGA). The proposed architecture works with 171 look-up tables (LUTs) and generates interpolated pixel at 0.402 ns. Further, clamp filtering technique is added as a pre-filter to increase the image quality. The experimental results show that the proposed FOPCI produces higher peak signal to noise ratio (PSNR) as 69.17 dB by comparing with other interpolation techniques. Thus, area efficient first order polynomial convolution image interpolation architecture is created by reducing number of components and by improving interpolated image quality, which is intended for visual communication systems with high image quality. Image

KEY WORDS
image scaling, weighting coefficient, computational complexity, FPGA, convolution interpolation

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INTRODUCTION

Low bandwidth and restricted channels are one of the supreme stimulating concerns that all the nations in this world is facing. Ever since signals and data to be directed via a channel are obtainable in vast expanse and restricted volume of band is allocated to every nation, multimedia data needs to be compressed at the source and expand at the destination so as to send multiple data. This compression and expansion may cause distortion of data and occasionally even produces false reconstruction at the destination. If the network is wireless, the condition flush develops poorer. Much noise enters the network along with the signals and attempt to depreciate the signal. If a digital image is directed via a wireless network it has to be compressed at the transmitter due to limited channels. At the receiver it may possibly get distorted due to the occurrence of noise and through image expansion it might get differed from its unique form. Several features of images are barely visible to eye, they must be frequently transformed before display. Image enhancement is a technique for improving the image quality which ensures increase in image vision and makes the image adjust to be treated by computer. It improves some data inside the image selectively and limits the other ones. To rebuild or expand the image to become the original form, interpolation is done [1].

Image interpolation is an art of rescaling low-resolution image to a high-resolution version, and it has become a very active area of research in image processing. The interpolation that estimates the intermediate values of a set of discrete samples has been used extensively in the field of digital photography, computer vision, computer graphics, medical imaging, consumer electronics like digital television and personal mobile devices and it also used in visual information processing system [2]. Interpolators based on approximations of the ideal sinc kernel (pixel replication, bilinear, bi-cubic, and higher order splines) are commonly used for their flexibility and speed, but these approaches frequently contribute to blurring and ringing artifacts, jagged edges and unnatural representation of the curves of constant intensity in processed images.

In recent years, many high-quality adaptive image interpolation techniques have been proposed. These novel methods greatly improve image quality by some efficient techniques, such as bilinear interpolation with sharpening spatial filter [3], linear space-variant edge detector [4], edge-weighted scheme [5] and pre-filters [6]. These methods produce better image but the major drawbacks is computational complexity, a large chip area and high hardware cost. Additionally, in past decade, many non-adaptive interpolation techniques have also been developed to reduce the chip area such as bi-cubic [7], extended linear [8], linear [9] efficient bi-cubic [10], piecewise linear convolution [11] first order polynomial convolution interpolation [12] and region of interest method [13]. Non-adaptive image interpolation performs in a fixed pattern for every pixel and this technique is fixed the irrespective of the input image features [14]. This work deals with polynomial convolution interpolation with first order and low complexity weighting coefficient generator to reduce the chip area. Furthermore, this work concentrates on improving the image quality by using clamp filter.

Reconfigurable hardware like FPGA is widely used for rapid prototyping digital signal processing [15] and digital image processing. Very large scale integration (VLSI) architecture is designed and evaluated by

using FPGAs [16]. This work presents FPGA implementation of low computation complexity image interpolation based on the first order polynomial convolution kernel [12].

The remaining portion of this paper is organized as follows. Section 2 analyses different non-adaptive and adaptive image interpolation techniques, Section 3 describes that the interpolation based on the first order polynomial convolution kernel, Section 4 deals with FPGA implementation of the proposed low-complexity image interpolation, Section 5 provides experimental analysis of both existing first order polynomial and the proposed interpolation methods and Section 6 presents the conclusion.

RELATED WORKS

In non-adaptive image interpolation methods, certain computations are performed indiscriminately to the whole image for scaling regardless of its contents. Among the various non-adaptive interpolation algorithms, the nearest neighbour and bilinear interpolations are simple [17], but, they have undesirable blurring and block effects. Polynomial interpolation methods have been studied quite extensively in the image processing literature of the fast three decades [18]. An example of such methods is cubic convolution interpolation method. The cubic convolution interpolation function is more accurate than the nearest neighbour or linear interpolation methods [19]. For convolution based interpolation, the sinc-approximating kernel with higher-degree spline can produce better results at an increase in computational cost [20].

FPGA-based bi-cubic interpolation is proposed by Maganda and Estrada [7] for digital image scaling. The hardware architecture of this interpolation is implemented on Xilinx Virtex-II FPGA with 890 configurable logic blocks (CLBs). An efficient bi-cubic convolution interpolation architecture is presented by Lin et al[10], which decreases the computational complexity of generating coefficients. The hardware architecture of this bi-cubic convolution interpolation operates at 279 MHz with 30643 gates in a 498×498 μm^2 chip. The FPGA implementation needs only about 437 logic blocks but the bi-cubic algorithm [7] requires about 890 logic blocks.Pang et al [21] proposed a bi-cubic interpolation with an adaptive sharpening filter to reduce the blurring effects. The VLSI architecture of this interpolation utilizes 695 logic elements and obtains an average PSNR increase of 1.5 dB. A novel image scaling algorithm is presented by Huang et al [5] using convolution interpolation kernel with a bilateral error-amender and an edge-weighted scheme. This provides average PSNR of 43.31 dB for image enlargement.VLSI architecture of an area efficient convolution based image interpolation is presented by Moses and Selvathi [16]. This work presents FPGA implementation of convolution kernel-based interpolation for digital image scaling. This method produces the PSNR of 51.55 dB for the image of 'aerial' (512 x 512) for the up-scaling ratio of 2 after 1/2 downscaling. The FPGA implementation of this method requires 336 LUTs. Lee & Park [22] presented a high performance low area up-scaling using Lagrange interpolation, which produces higher visual quality on interpolated image over the bi-cubic interpolation. This method uses sharpening filter technique to improve the quality of the interpolated image by enhancing edge regions. This method achieves an average SSIM as 0.8406 by using edge detection and sharpening filter with Lagrange interpolation for 2 x scaling. However, it achieves only 0.7006 SSIM for 3x scaling.

An extended linear image interpolation for real time applications is proposed by Lin et al [8]. The hardware architecture of this interpolation is implemented on the Virtex-II FPGA, and implemented with TSMC 0.13μm standard cell library. The high speed architecture is simulated at 267 MHz operating frequency with 26200 gates in a 452×452 μm^2 chip is capable of producing digital image interpolation for high definition television (HDTV) in real-time. A linear interpolation is proposed by Lin et al [9], which reduces the efforts of generating coefficient. The hardware architecture of this algorithm is also implemented on Virtex –II FPGA with 379 logic blocks (LBs). This architecture wants about 26200 gates and achieves higher PSNR (33.12 dB) for the test image (airplane). A piecewise linear convolution interpolation, with third-order approximation, is presented by Lin et al [11]. The number of CLBs used by Virtex – II FPGA for bi-cubic (Maganda and Estrada 2005) and this algorithm are 437 and 393 respectively. This interpolation scheme provides higher PSNR (49.53 dB) than the bi-cubic (46.38 dB) for the test image (airplane) of scaled from 3/4 downscaling after 4/3 upscaling. An efficient extended linear image interpolation is implemented by Lin et al [23] by using Virtex-II FPGA and TSMC 0.13 technologies. This uses 25980 gates at 267 MHz in TSMC 0.13 and the FPGA implementation uses only about 379 CLBs but the bi-cubic [7] needs about 437 CLBs. This method provides higher PSNR (35.29 dB) than the bi-cubic [7] for the test image (tank) for 3/2 upscaling after 2/3 downscaling. Huang & Chang [24] presented an adder-based stepwise linear interpolation (ABSI) for digital signal processing. The hardware architecture of this method uses simple operators such as compare, shift and add. This technique achieves similar interpolation quality with conventional multiplier-based linear interpolation (MBLI), but it requires less area and consumes low power. This method achieves the highest PSNR of 32.34 dB.

An adaptive interpolation technique is presented by Chen et al [6] using clamp filter and a sharpening spatial filter as pre-filters to reduce the blurring and aliasing effects of the bilinear image interpolation algorithm. This architecture is implemented on FPGA, TSMC 0.18μm and TSMC 0.13μm technologies. This scheme utilizes 9.28 K gates and 9.27 K and 9.28 K gates on FPGA and on TSMC 0.18μm and TSMC

0.13µm respectively. This method improves average image quality by 0.42 dB over other adaptive interpolation techniques. VLSI architecture of a high quality image scalar is proposed by Chen [3] using a sharpening spatial filter, a clamp filter, and a bilinear interpolation technique. The VLSI design of this scalar can operate at 280 MHz with 6.08-K gate counts. This work can also achieve an average PSNR of 28.54 dB for image scaling. Another low complexity adaptive edge-enhanced image interpolation technique is also presented by Chen [4] using bilinear interpolation and sharpening spatial filter as a pre-filter and a linear space-variant edge catcher. This work achieves an average PSNR of 34.26 dB for image scaling. This PSNR value is higher than the previous Chen's proposal [3] due to the usage of adaptively edge catching technique. The VLSI architecture of this interpolation uses 6.67 K gate count and achieves about 280 MHz by using the TSMC 0.13 µm VLSI technologies.

Li and Yu [13] presented a block region of interest method for FPGA implementation of image interpolation algorithm. In this method, a block region of interest is used for large image reconstruction using 2D sinc interpolation. The hardware architecture of this method is realized by pipelining on Virtex 7 FPGA with 187680 LUTs, 288272 registers. First-order polynomial convolution interpolation (FOPCI) for real-time digital image scaling is presented by Lin et al [12]. The kernel of the proposed method is built up of the first-order polynomials and it approximates the ideal sinc-funtion in the interval [-2, 2]. The architecture is implemented on the Virtex-II FPGA, and the VLSI architecture has been designed and implemented with the TSMC 0.13 µm standard cell library. The number of adders and subtractors used to generate weighting coefficients in the architecture is less than that of bi-cubic interpolation [7].

The proposed FOPCI uses low complexity WCG to reduce the number of arithmetic elements in the interpolation. The various area dependent parameters like look-up tables (LUTs), configurable logic blocks (CLBs) of earlier low complexity interpolator for multimedia applications [5], [10] and [16], existing FOPCI [12] and proposed architectures for visual communication systems are evaluated by using Xilinx system generator. Further, it improves the image quality by using clamp filter.

First order polynomial convolution interpolation

The block diagram of the hardware architecture for digital image scaling is shown in [Fig. 1], which includes Coordinate Calculation Unit, Memory Bank, weighting co-efficient generator (WCG), Vertical and Horizontal Interpolation units and Virtual Pixel Buffer [12]. The coordinate calculation unit includes interpolated coordinate accumulator, row/column address calculator and vertical and horizontal distance calculator. The coordinate of the interpolated point Q (x_n, y_m) is obtained in the interpolation coordinate calculator. In the circuit of row/column address calculator, the operation of vertical or horizontal address orientation is controlled by the vertical/horizontal signal. This signal determines the vertical (y_m) and the horizontal (x_n) coordinates. If the signal vertical/horizontal is vertical, then the row addresses and the vertical interval s_v can be obtained. Otherwise, the column addresses and the horizontal interval h_v can be found. The vertical distance calculator calculates the distance between the source pixel and the virtual interpolated pixel. Similarly, the horizontal distance calculator calculates the distance between the virtual interpolated pixel and the final interpolated pixel.

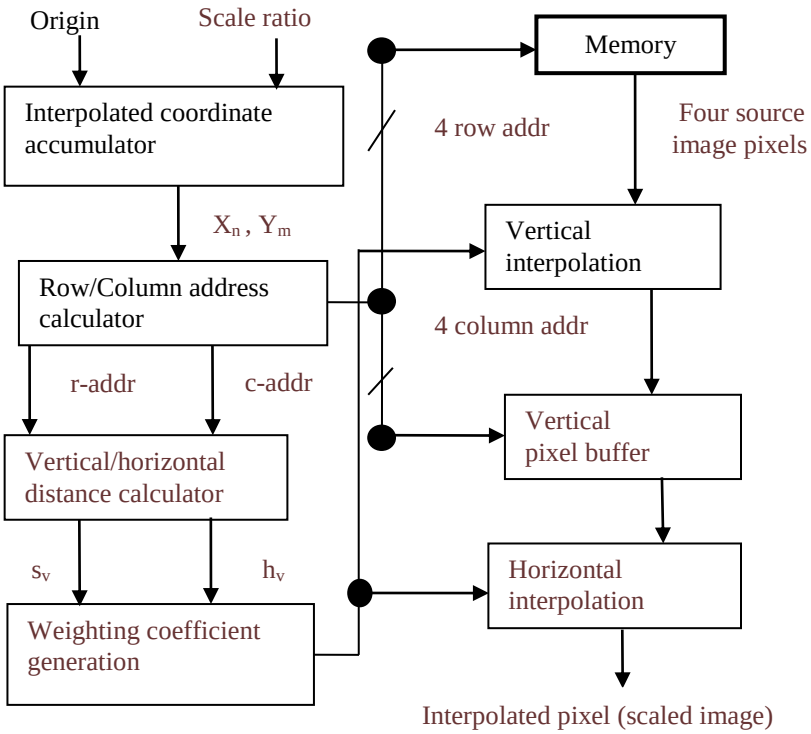

Fig. 1: Block diagram of the hardware architecture for digital image scaling

The most important computation in convolution-based scaling is the calculation of interpolation weighting coefficients. By using low area WCG [25] an area efficient FOPCI can be implemented. [Fig. 2] shows the vertical/horizontal interpolation unit used for image scaling. The vertical interpolation unit performs interpolation in column wise manner to produce virtual pixel. The horizontal interpolation unit performs interpolation for these virtual pixels to produce interpolated pixel. The virtual pixels created from vertical interpolation are stored in the virtual pixel buffer, as shown in [Fig. 1], they areaccessed in the process of horizontal interpolation.

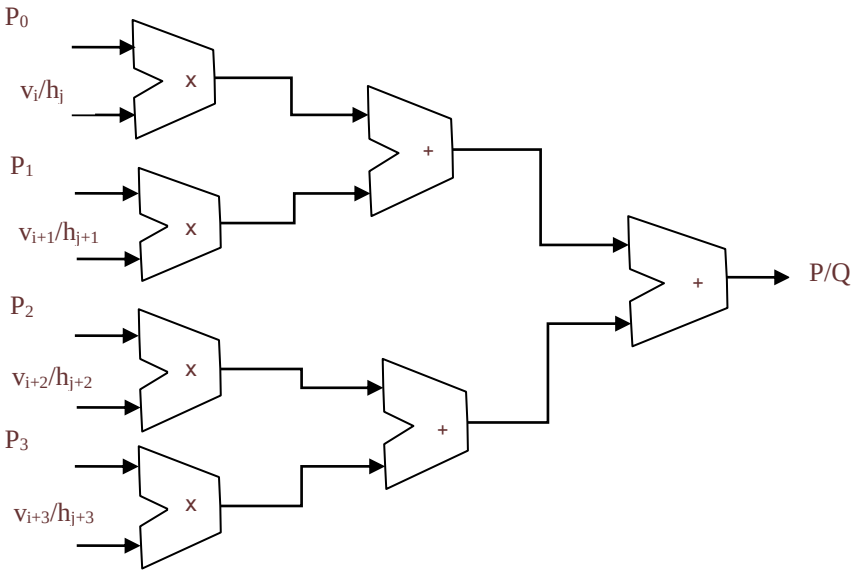

Fig. 2: Vertical/Horizontal Interpolation unit.

As shown in [Fig. 2]the vertical and horizontal interpolations have the same operation, but they have to execute in parallel to accelerate scaling speed.

PROPOSED FOPCI

A low complexity hardware for image interpolation is proposed by reducing the computational complexity of weighting coefficient generator. To verify the performance of the proposed hardware architecture of image interpolation, the interpolation circuit is connected with image preprocessing and post processing circuit as shown in [Fig. 3].

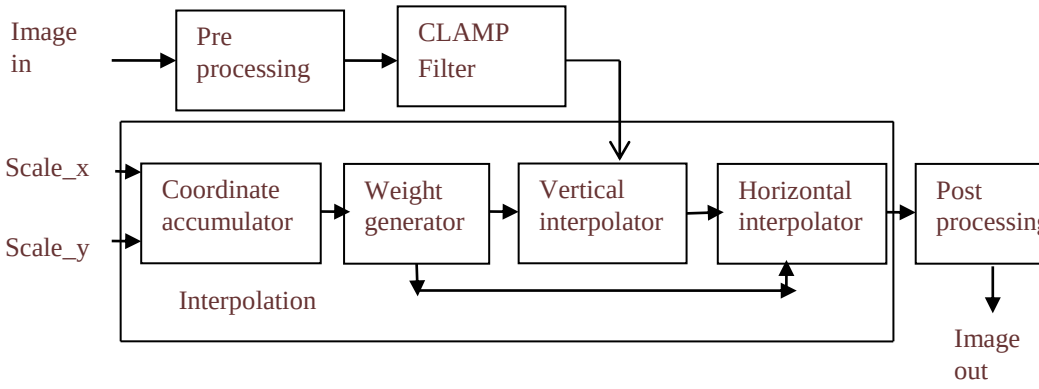

Fig.3: Block diagram of the proposed interpolation method.

Image preprocessing in Matlab simulink helps in providing input to FPGA as specific test vector array which is suitable for FPGA bitstream compilation using system generator [26].

To reduce the area of the VLSI architecture of FOPCI [12], an optimized design of weighting coefficient generator (WCG) is used. The most computational effort in the proposed WCG is the reduction of number of arithmetic elements. The simplified WCG includes only two adders, three dividers and four subtractors [25]. The proposed filtering technique for the improvement of interpolation is implemented by Clamp Filter as shown in [Fig. 3]. Clamp filter is a low-pass filter which is used for smoothing discontinuous edges and decreasing block effect caused by the interpolation method. An example of a 3x3 kernel for a clamp filter is shown in equation (1).

$$Kernel\ c = \begin{matrix} 1 & 1 & 1 \\ 1 & C & 1 \\ 1 & 1 & 1 \end{matrix} \quad (1)$$

where, C is a clamp parameter that can be set according to the characteristics of the images. The clamp filter is stable when the clamp parameter C is varied between 6 and 30 [6]. The new pixel value is computed based on the array of the clamp fitter as

$$P'(i,j) = \left[P(i,j) * \begin{matrix} 1 & 1 & 1 \\ 1 & C & 1 \\ 1 & 1 & 1 \end{matrix} \right] \div (C \div 8) \quad (2)$$

RESULT AND DISCUSSION

The performance of scaling algorithm is evaluated based on two categories such as quality/quantitative measure and hardware performance measure. Quantitative measure specifies the quality of the interpolated image based on PSNR. The PSNR is estimated by using equation (5) [6].

$$MSE = \frac{1}{MN} \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} [P(i,j) - P'(i,j)]^2 \quad (3)$$

where, MSE is the mean square error M and N are the width and height of the actual input image. P (i,j) is original input image and P'(i,j) is interpolated output image.

$$PSNR = 10 \log_{10} \frac{MAX^2}{MSE} (4)$$

When the pixels are represented by eight bits per sample, the maximum value of each pixel (MAX) is 255. Therefore, the quality tends to be expressed in dB with a PSNR given as

$$PSNR = 10 \log_{10} \frac{255^2}{MSE} (5)$$

The quality measure of various interpolation methods is evaluated by using MATLAB. For testing the quality of scaling algorithms, images from USC-SIPI database of size (512 × 512) are selected. [Fig. 4] shows the test images from the USC-SIPI database considered for experimentation. The images are tank, girl, pepper, pirate, livingroom, boat, house, san-diego (aerial), pepper and stream and bridge. [Fig. 5] shows the sample interpolated image. [Table 1] lists the PSNR of different interpolation methods respectively.

Fig. 4: Input images considered for experimentation.

(a) Input image

(c) Upscaled image by 2

Fig. 5: Sample interpolated image.

Table 1: PSNR of various interpolation methods for upscaling ratio of 2 after 1/2 downscaling

Image	Interpolation Methods					
	Bicubic [10]	Bilinear [4]	Convolution based [5]	Bicubic [21]	FFOPCI [12]	Proposed
Tank	56.23	56.74	65.31	68.34	68.50	69.17
Girl	55.13	50.56	64.63	67.15	67.46	67.91
Pepper	53.28	49.22	62.21	64.60	64.95	65.11
pirate	54.67	46.31	58.21	61.33	61.75	62.17
Living room	52.46	45.00	55.17	58.08	58.54	59.09
Boat	52.17	44.54	55.92	58.90	59.35	59.77
House	49.25	40.34	52.97	55.86	56.35	56.88
San-diego	49.59	39.41	50.91	54.24	54.78	55.48
Mandrill	50.78	41.89	50.72	53.57	53.79	54.22
Stream and Bridge	48.93	41.27	49.71	52.75	52.99	53.61

The results shown in [Table I] demonstrate that the PSNR value is high (69.17 dB) for the test image 'tank' by using the proposed method. To evaluate the performance of the proposed image interpolation, the proposed architecture and the existing architectures are simulated, synthesized and implemented for Virtex xc6 vsx315tff1156-3 by using MATLAB Simulink and Xilinx ISE 14.5. [Table 2] shows the comparison of different device utilization factors of previous low complexity interpolation methods and the proposed FOPCI methods.

Table 2: Comparison of VLSI design parameters of proposed methods with other interpolation techniques

Parameters	Interpolation Methods					
	Bicubic [10]	Convolution based [5]	Convolution based [16]	FFOPCI [12]	Proposed A (without filter)	Proposed B (with filter)
Target device	Virtex xc6 vsx315tff1156-3					
Number of LUTs	198	364	336	191	171	260
Number of LUTs used as logic	175	351	330	176	147	213
Number of LUT flipflop pairs used	235	387	336	192	137	137
Number of occupied slices	63	102	84	74	57	87

Based on [Table 2], the proposed FOPCI without filter utilizes only 171 LUTs, which is much less than the previous works FFOPCI [12], Convolution based [5] and [16] and bicubic [10]. Further, the proposed FOPCI with filter utilizes only 260 LUTs, which is much less than the previous low complexity algorithms [5] and [16]. Comparing the proposed two methods, the method B costs 89 LUTs more than method A due to an additional clamp filter. However, it increases the quality by over 0.66 dB. To encapsulate, this work contributed in designing high-performance and high quality interpolation architecture of VLSI circuit for many visual communication systems.

CONCLUSION

This paper proposes an area efficient VLSI architecture of cubic convolution kernel-based interpolation for digital image scaling. The operation of the proposed architecture without filter requires five additions, four subtractions four multiplications and three divisions. Therefore, the number of arithmetic elements in the proposed architecture is much less than the other interpolation methods. Further, the proposed architecture with clamp filter increases the interpolated image quality with reasonable amount of LUTs. Consequently, the proposed VLSI architecture has solved the problem of computation complexity for generating weighting coefficients for image interpolation and furthermore, simplified the hardware for FPGA implementation and reduced the chip area. Additionally, the image quality is improved by using clamp fitter to reduce block effects of the interpolation. Thus, the proposed work is an area efficient high quality image interpolation for many compact visual communication systems.

CONFLICT OF INTEREST
There is no conflict of interest.

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None

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