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THE EXPERIMENTAL VERIFICATION OF BRIDGELESS TAPPED INDUCTOR SEPIC CONVERTER FOR BLDC MOTOR DRIVE APPLICATIONS

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ABSTRACT

Background: *This paper introduces a power factor corrected bridgeless tapped inductor SEPIC (BL TI-SEPIC) converter-fed brushless direct current (BLDC) motor drive in the form of a cost-economic solution for high-power applications.* ***Methods:*** *A mechanism of speed control of the BLDC motor through the control of the dc link voltage of the voltage source inverter (VSI) is exploited with a single voltage sensor.* ***Results:*** *A BL TI-SEPIC converter is presented that provides the removal of the diode bridge rectifier, thereby minimizing the conduction losses related to it.* ***Conclusions:*** *A BL TI-SEPIC converter is modelled to be operated in discontinuous current mode (DCM) to yield an intrinsic PFC at ac mains.* ***Applications:*** *The performance of the newly introduced driver is investigated under speed control with enhanced power quality at ac mains; in addition the validation of the BLDC driver proposed is done experimentally over a designed prototype.*

KEY WORDS

INDEX TERMS
Brushless Direct Current (BLDC), Power Factor Correction (PFC), Electronic Commutation, *Discontinuous Current Mode (DCM)*

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INTRODUCTION

Resourcefulness and being cost-economic are the importantchallenges in developing low-power motor drives aiming at household applications like fans, water pumps, blowers, mixers, etc. The usage of the brushless direct current (BLDC) motorin these applications is getting popular because of features likebetter efficiency, greater flux density per unit volume, lesser requirements for maintenance, and lesser electromagnetic-interference issues[1,2].

A BLDC motor consists of three phase windings on the stator in addition to permanent magnets on the rotor. The BLDC motor isalso referred to as an electronically commutated motor since an electronic commutation dependent on rotor position is employed instead of a mechanical commutation that has demerits such as sparking and wear and tear of brushes and commutatorassembly [3, 4].

A BLDC motor, while beingpowered by a diode bridgerectifier (DBR) with a large value of dc link capacitor obtains peaky current that can result in a THD of supply current of the magnitude of 65% and power factor as less as 0.8 [5]. Therefore, a DBR, which is followed by a power factor corrected (PFC) converter is used for boosting the power quality at ac mains. For the purpose of reducing the losses of the DBR, many bridgeless (BL) PFC rectifiers have been introduced for enhancing the rectifier power density and/or reduces noiseemissions [6], [7]by means of the soft switching techniques.

The traditionalBL PFC method of the BLDC motordrive uses a pulsewidth-modulated voltage source inverter(PWM-VSI) for speed control along with a continuous dc link voltage.This givesgreater switching losses in VSI since the switchinglosses are increasedin the order of a square function of the switching frequency. Since the speed of the BLDC motor is in direct proportion with thedc link voltageapplied, the speed control is attained bythe variable dc link voltage of VSI. This permits for the fundamentalfrequency switching of VSI (i.e., electronic commutation) and renders reduction in the switching losses.

PROPOSED TOPOLOGY

This studydemonstrates a newbridgeless SEPIC converter in addition to the tapped inductor (TI) model (BL TI-SEPIC)that has a wide gain range for the BLDC motor drive applications. The schematic diagram of the proposed BL TI-SEPIC converteralong with the conventions of the circuit variables which are followed is shown in [Fig. 1].

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The converter circuit proposed comprises of an input inductors L_1 and L_2; the main switches S_1 and S_2; intermediate capacitors $C_1$and C_2; then a voltage multiplier cell is also included in the circuit, consisting of C_m, D_{m1} and D_{m2}; a Tapped Inductor (TI) of L_p, L_s; and a charge pump is also included in the circuit whichcontainsC_3, D_1 and D_0, whichfeeds an output filter capacitor, C_0, and finally a voltage source inverter (VSI) fed BLDC motor drive.

In the proposed topology, the use of bridgeless configuration will reduce the losses corresponding to conduction and the voltage multiplier cell will then have a maximization of the gain and reduce the s witch voltage stress. Hence, this novel topology boosts the efficiency on an overall. The proposed converter exploits two unidirectional switches ($S_1$and S_2). Switch $S_1$is turned ON/OFF during the positive half-line

cycle with the current flowing back to the source through the diodeD_p. During the time span of the negative half-line cycle, switch $S_2$is switched ON/OFF and then the current flows back passing through the diodeD_n. Moreover, the two power switches $S_1$and S_2can be fed by the same control signal whichassists in simplifying the control circuitry considerably.

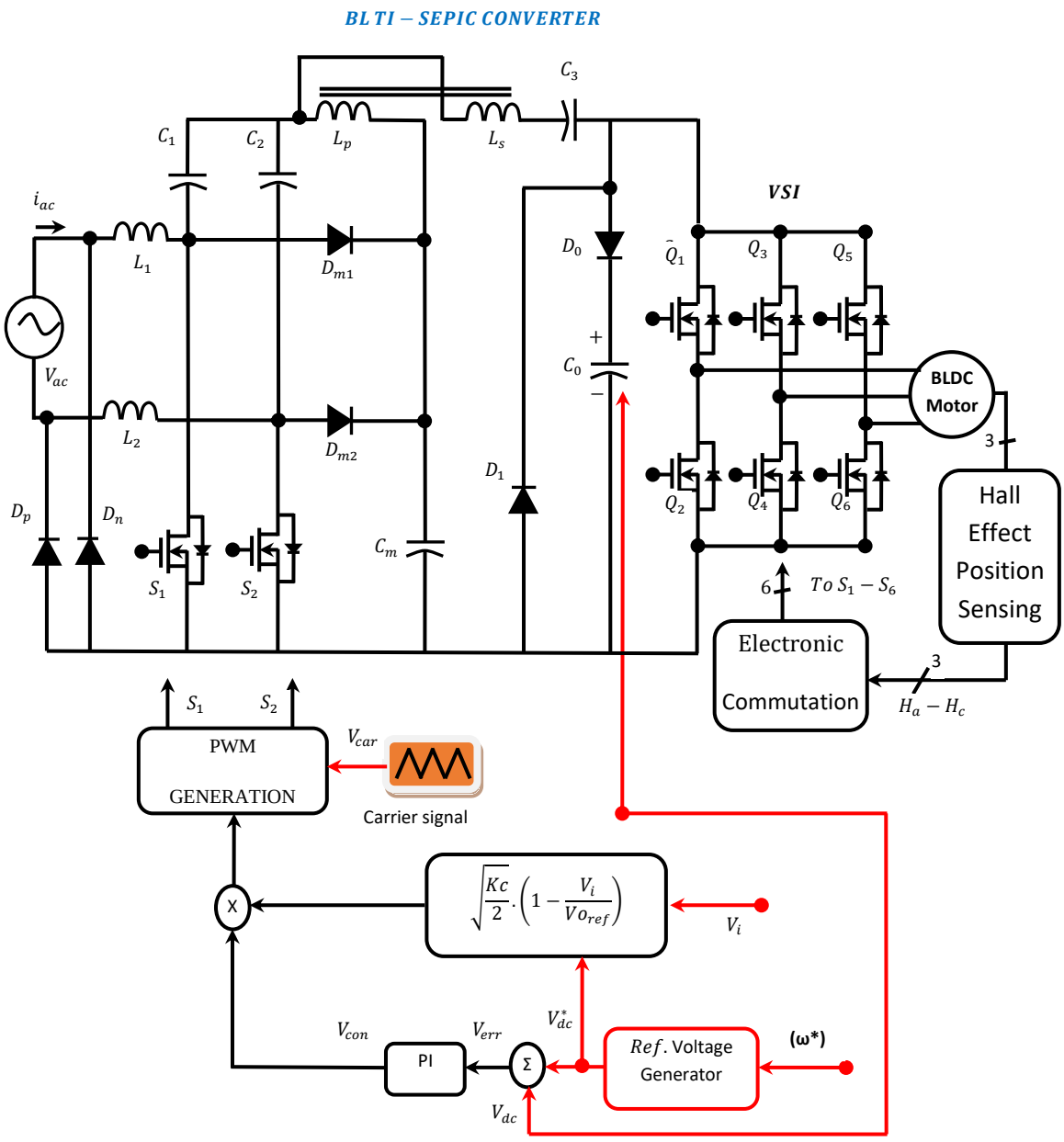

Fig.1: Schematic diagram of BL TI-SEPIC converter

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Voltage follower approach

As illustrated from the [Fig. 1], a single voltage control loop (voltage follower mechanism) is employed for the BL-TI SEPIC converter. A reference dc link voltage (V_{dc}^*) is generated as

$$V_{dc}^* = k_{volt} \times \omega^* \quad (1)$$

where$k_{volt}$and ω^*indicate the respectivethe voltage constant and the reference speed of the motor.
The voltage error signal(V_{err}) is produced by means of a comparison between the reference output voltage(V_{dc}^*) and the output voltage sensed (V_{dc}) expressed as

$$V_{err}(k) = V_{dc}^*(k) - V_{dc}(k) \quad (2)$$

In which (k) indicates the(k^{th}) sampling instant. This error voltage signal (V_{err}) is given as input to the voltage proportional–integral (PI) controller for generating a controlled output voltage (V_{con}) as

$$V_{con}(k) = V_{con}(k-1) + k_p\{V_{err}(k) - V_{err}(K-1)\} + k_i V_{err}(k) \quad (3)$$

In which k_p and k_i stand for the corresponding proportional and integral gains of the voltage PI controller.

Electronic commutation

An electronic commutation of the BLDC motor comprises of the correct switching of VSI such that a symmetrical dc current is received from the dc link capacitor for 120◦ and thereafterpositionedsymmetrically at the centre of each phase. A Hall-effect position sensor is used for the sensing of the rotor position with a 60◦span which is required for the electronic commutation of the BLDC motor.

Table 1: Switching states based on hall effect position signals

θ^0	HALL SIGNALS			SWITCHING STATES					
	H_a	H_b	H_c	S_1	S_2	S_3	S_4	S_5	S_6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

A line current is got from the dc link capacitor whose magnitude is in accordance with the dc link voltage applied, back electromotive forces, resistances, and self-inductance and mutual inductance corresponding to the stator windings. [Table 1] shows the different switching states of the VSI that powers a BLDC motor based on the Hall-effect position signals (Ha – Hc).

EXPERIMENTAL EVALUATION

The performance of the newBL TI-SEPIC converter fed BLDC motor drive application is validated experimentally on a developed hardware prototype as illustrated in [Fig. 2]. A developed hardware prototype chieflyconsists of 16 bit digital signal controller (dsPIC30F4011), MOSFET driver circuit for front end BL TI-SEPIC converter and VSI switches, Hardware arrangement of BL TI-SEPIC converter and VSI for power factor correction (PFC) and speed control operationcorrespondingly.

MOSFET driver circuit for BL TI-SEPIC converter and VSI switches

The switching signal for a MOSFETgenerallygets generated by means a logic circuit or a microcontroller that offers an output signal which isusuallywithin a few mill amperes of current. As a result, a MOSFET, directly powered by such a signal would not be switching very fast, along with respectivehuge power loss. During the switching, the gate capacitor of the MOSFET may obtain current so rapidly that it creates a current overdraw in the logic circuit or microcontroller, leading to overheating, that again results in a permanent damage or even wholly destroy the chip. In order to avoid this, a MOSFET driver is placed between the microcontroller output signal and the power MOSFET.The MOSFET driver unit generallyconsists of transistor BC547, optocoupler 6N139 and MOSFET driver IC DS0026 as illustrated in [Fig. 3].

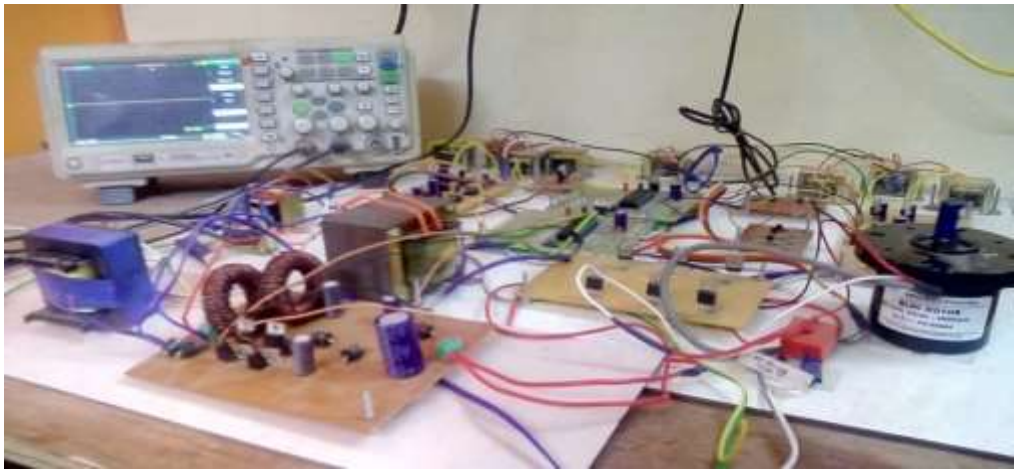


Fig.2: Proposed BLDC motor driver prototype test setup

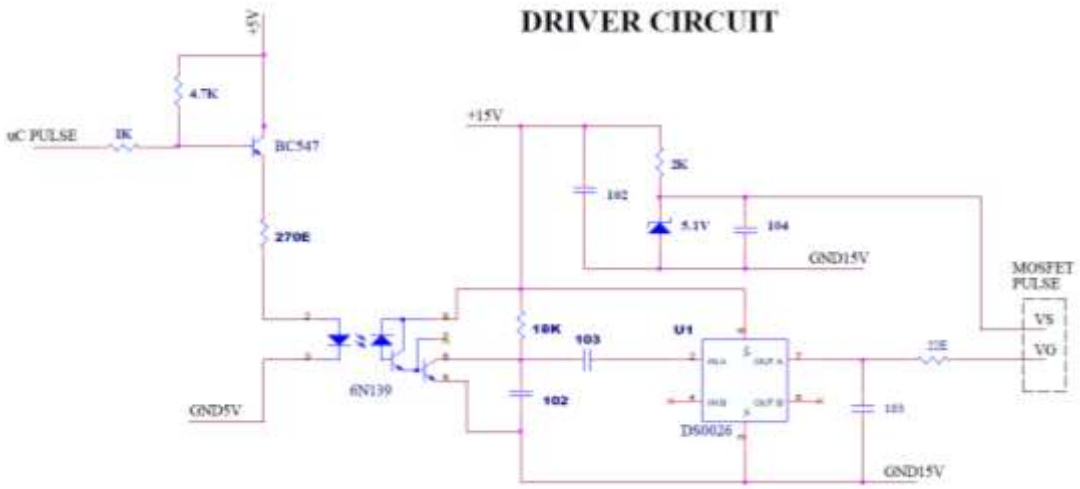
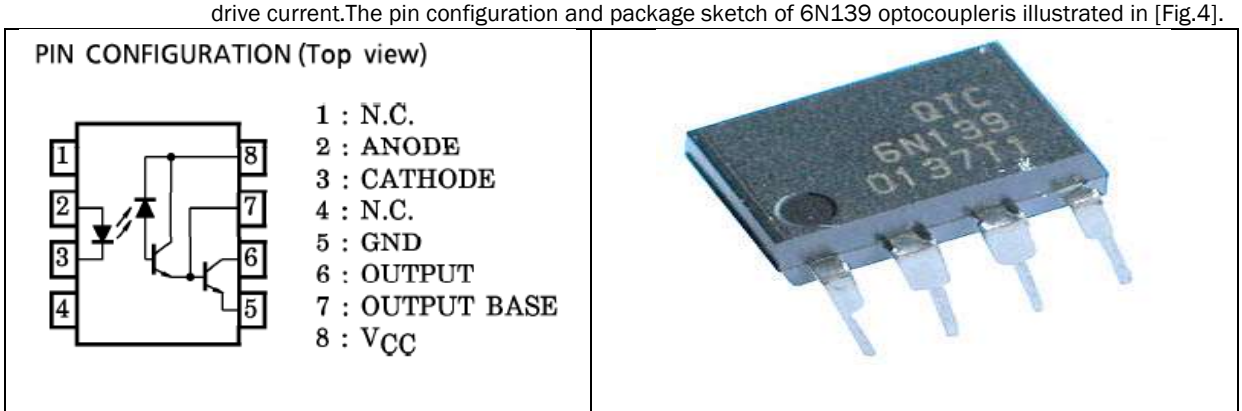


Fig.3: MOSFET driver circuit

In MOSFET driver unit BC547 is generallyutilized for the amplification of current. It is an NPN bi-polar junction transistor. A transistor, symbolic for transfer of resistance, in which a small current at its base controls a bigger current at the collector & emitter terminals. BC547 is typicallyutilized for the purposes of amplification and switching. Its maximum current gain is of 800.

The transistor terminals need a constantdc voltage to be operated in the desired region of its characteristic curves. This is called as biasing. It is employed in common emitter configuration for amplifiers.

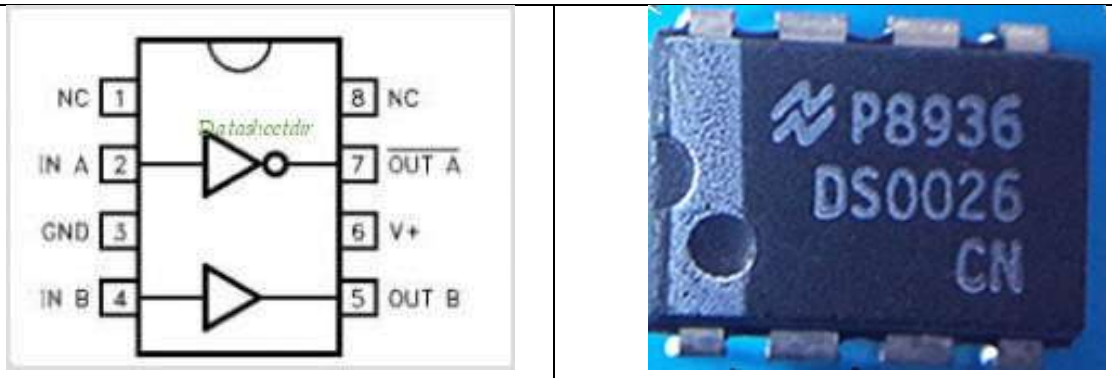
In a similar manner, the optocoupler TOSHIBA 6N139 comprises of anGaAlAs infrared emitting diode which is coupled with a split-Darlington output configuration. A high speed GaAlAs infrared manufactured with a distinct liquid phase epitaxial (LPE) junction, has the characteristic of rapid rise and fall time at low drive current.The pin configuration and package sketch of 6N139 optocoupleris illustrated in [Fig.4].



(a) Pin diagram of 6N139 (b) Package sketch of 6N139

Fig. 4: Optocoupler (6N139) schematic diagram

In MOSFET driver unit, the part played by driver IC DS0026 is its use for the maximization of the switching speed. DS0026is a cost economic monolithic high speed two phase metal oxide semiconductor (MOS) clock driver and interface circuit. This distinct circuit design gives very high speed operation along with the capability to drive huge capacitive loads. The device permits standard transistor-transistor logic(TTL) outputsand transforms them to MOS logic levels. DS0026 is bestowed with the features such as fast rise and fall times (20ns 1000 pF load), high output swing (20V) and high output current drive (∓ 1.5 Amps).The pin configuration and package sketch of driver IC DS0026 is illustrated in [Fig. 5].



(a) Pin diagram of DS0026 (b) Package sketch of DS0026

Fig. 5. Driver IC (DS0026) schematic diagram

Hardware arrangement

A PFC BL TI-SEPIC converter is modelled in order to operate indiscontinuous conductionso that the current in inductors (L_1 and L_2) tends to becomediscontinuous in a switching period. For a BLDC motor of powerrating 30 W (entire specifications of the BLDC motor are provided in the [Table 2].Corresponding to a huge variation in the dc link voltage (speed control), the output voltage is controlled ranging from a low value of 16 V (Vout_l) to the maximum value of 24 V (Vout_m). The average voltage that appears at the input (Vin) is decided by equation (4)[8].

$$Vin = \frac{V_{ac} \times \sqrt{2} \times 2}{\pi} = \frac{12 \times 1.414 \times 2}{3.14} \cong 10.80\ V$$

Where (V_{ac}) indicates the Rms value of supply voltage.
The speed control of BLDC motor is got by changing the duty ratio (d) in the range of minimum (d_{mn}) to maximum (d_{mx}) asexpressed by equation (5 to 7)[9].

$$d = \frac{Vout}{Vin + Vout}$$

$$d_{mn} = \frac{Vout\_l}{Vin + Vout\_l} = \frac{16V}{10.80\ V + 16\ V} \cong 0.59$$

$$d_{mx} = \frac{Vout\_m}{Vin + Vout\_m} = \frac{24V}{10.80\ V + 24\ V} \cong 0.689$$

The minimum and maximum duty ratios are computed as 0.59 and 0.69 correspondingly.

In order to have the theinput inductance (L_1 and L_2) valueestimated, and for operation in buck and boost mode in the BL TI-SEPIC converter, theequation (8 and 9)[10] is provided

$$L_1 = L_2 = \frac{(Vout\_l)^2}{Pout\_l} \times \frac{(1 - d_{mn})^2}{2 \times f_s}$$

$$L_1 = L_2 = \frac{(16)^2}{14.4} \times \frac{(1 - 0.59)^2}{2 \times 10000} = 149.42\mu H$$

Where(f_s)refers to the switching frequency, (d) indicates the duty ratio. So, the value of ($L_1$and L_2) is computed at the minimum duty ratio of (d_{mn})so that the converter works in DCM even at conditions of very

low duty ratio. At minimum duty ratio, i.e., the LED Lamp that operates at 16 V (Vout_l), the power (Pout_l) is provided as 14.4 W. The values of input inductances $L_1$and L_2 are considered to be less than 1/10th of the minimum critical value of inductance to guarantee a deep DCM condition [11].Therefore, the input inductors L_1 and L_2 are chosen to be around 1/10th of the critical inductance and are considered as14 µH.

The value of the in-between capacitors (C_1, C_2, C_3 and C_m) is computed for the maximum duty ratio (d_{mx}) asprovided by equation (10 and 11) and is expressed as [9]

$$C_{1,2,3,m} = \frac{d_{mx} \times V_{cap}}{2 \times f_s \times \frac{(Vout\_m)^2}{Pout\_m} \times \frac{\sim V_c}{2}}$$

Where ($V_{cap} = Vin + Vout\_m$) represents the voltage across the capacitors (C_1 or C_2 or C_3 or C_m), and the allowable voltage ripple ($\sim V_c$) is considered as 60% of (V_{cap}).

$$C_{1,2,3,m} = \frac{0.69 \times (10.80 + 24)}{2 \times 10000 \times \frac{(24)^2}{18.67} \times \frac{20.4}{2}} = 3.815\mu F$$

Therefore, the values of in-between capacitors (C_1 or C_2 or C_3 or C_m) are chosen to be 3.3µF.

The value of the coupled inductors (L_p and L_s) for the admissible ripple current ($\sim Iout\_mx$) in the coupled inductors, is considered to be 10% of output current ($Iout\_mx = 0.715$ A) is computed as [12] and expressed in equation (12 and 13).

$$L_p = \frac{d_{mx} \times Iout\_mx}{f_s^2 \times 16 \times Cint \times \frac{(\sim Iout\_mx}{2}}$$

Where (Cint) indicates intermediate capacitor value.

$$L_p = \frac{0.69 \times 0.715}{(10000)^2 \times 16 \times 3.815 \times 0.0398} = 2.03nH$$

Hence the values of coupled inductor(L_p) got is (2.03nH).Moreover, the coupled inductor (L_s) value is got on the basis of output voltage gain.
The output capacitors (C_0) value is got by the equations (14 and 15) for the minimum duty ratio expressed as [9]

$$C_0 = \frac{Iout\_mx}{\sim V_{out-min} \times \omega_l \times 2}$$

$$C_0 = \frac{0.733}{(0.03 \times 16) \times (2 \times 3.14 \times 50) \times 2} = 2371.94\mu F$$

Where (ω_l) indicates the angular frequency, permitted ripple voltage ($\sim V_{out-min}$) in the output capacitors (C_0), considered as 3%, therefore the output capacitors value of2200 µF is chosen.

Table 2: Proposed BLDC motor driver component specifications

S. No	BL TI-SEPIC converter fed BLDC motor driver component details	Operating values
1	Unidirectional N-Channel Power MOSFET (IRFZ44N) (S_1 *and* S_2) for PFC BL TI-SEPIC converter ($Q_1 - Q_6$) for VSI	50 V, 50 A
2	Input inductors (L_1 *and* L_2) Core type: "Round" Size : T45*26*15 ring Toroidal ferrite core	14 μH

	Copper gauge : "25"	
3	In-between capacitors (C_1 or C_2 or C_3 or C_m) Type: electrolytic	$3.3\ \mu F, 50\ V$
4	Schottky power diode(D_p or D_n or D_{m1} or $D_{m2}$$or$$D_1$ or D_0) Brand: Fairchild semiconductor Part no: SB550	50V, 5A
5	Coupled Inductors (L_p and L_s) Core type: "E-core" Size: E65*32*27 core Copper gauge: "19"	Ratio 1:2, Primary inductance value = $2.03nH$, Secondary inductance value = $6nH$
6	Output capacitors (C_0) Type: electrolytic Brand: nichicon	$2200\ \mu F, 50\ V$
7	Load: BLDC motor Model no: 2RB30AK	Dc voltage : 24V Power: 30W Speed : 3000 Rpm Torque: 1.2 Nm

RESULTS AND DISCUSSIONS

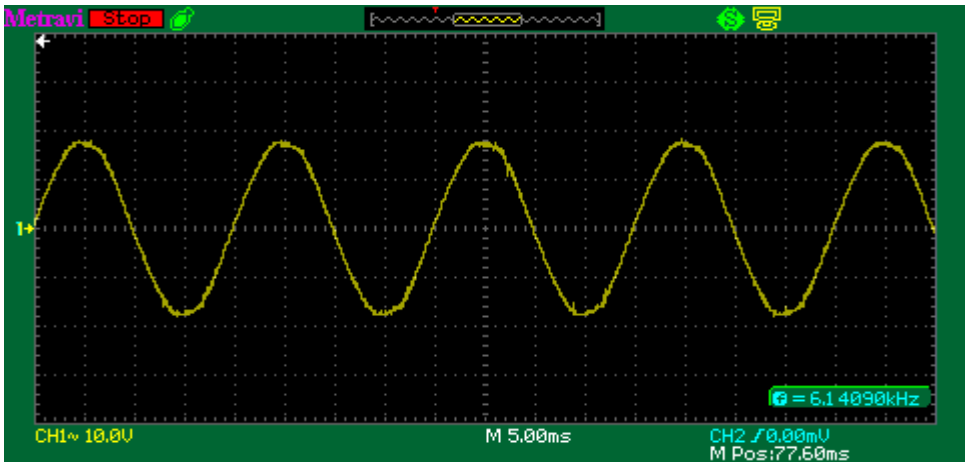
A digital signal controller dsPIC30F4011 controller is utilized for developing the novel PFC BL TI-SEPIC converter-fed BLDC motor drive. The required circuitry for separation between dsPIC30F4011 controller and gate drivers of solidstate switches is designed making use of the optocoupler 6N139. Aprefiltering and isolation circuit for the Hall-Effect sensor isalso designed for the sensing of the Hall-effect position signals. The input and output specifications of the new system experimental verification is illustrated in

Table 3: The Test results are studied in the sections that follow

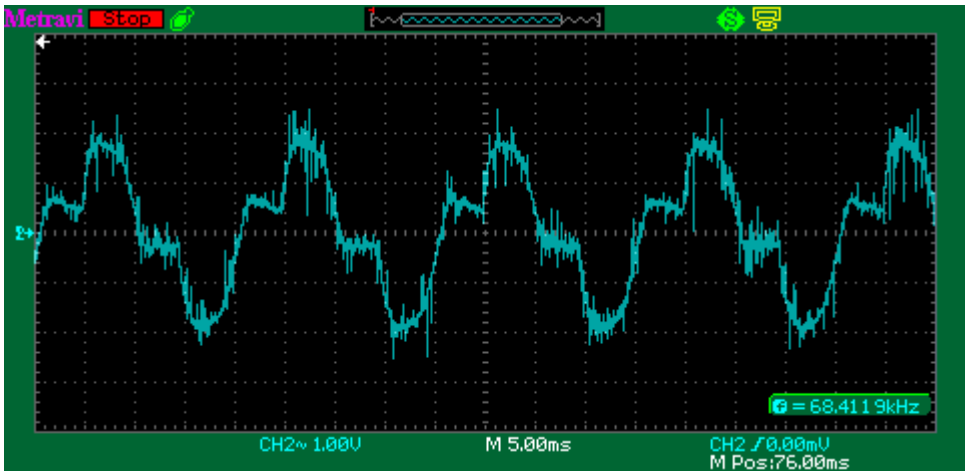
S. No	Input and output specifications of BL TI-SEPIC converter	values
	BL TI-SEPIC converter operates in minimum output voltage	
1	Input supply voltage	12.02 V (Rms)
2	Input supply current	1.2 A (Rms)
3	Input power	14.4 W (Rms)
4	BL TI-SEPIC converter dc output voltage ($Vout\_l$)	16 V
5	BL TI-SEPIC converter dc output current ($Iout\_l$)	0.831 A
6	BL TI-SEPIC converter dc output power ($Pout\_l$)	13.3 W
7	BLDC motor speed (no load condition)	1000 Rpm
	Power Factor	0.993
	BL TI-SEPIC converter operates in maximum output voltage	
8	Input supply voltage	12.02 V (Rms)

9	Input supply current	1.55 A (Rms)
10	Input power	18.67 W (Rms)
11	BL TI-SEPIC converter dc output voltage ($Vout\_m$)	24 V
12	BL TI-SEPIC converter dc output current ($Iout\_m$)	0.715 A
13	BL TI-SEPIC converter dc output power ($Pout\_m$)	17.16 W
14	BLDC motor speed (no load condition)	1500 Rpm
15	Switching frequency (f_{swh})	10kHz
16	Supply frequency	50Hz
17	Efficiency of BL-IZC operates in maximum output voltage (η_{max}%)	91.91%
18	Efficiency of BL-IZC operates in minimum output voltage (η_{min}%)	92.33%
	Power Factor	0.991

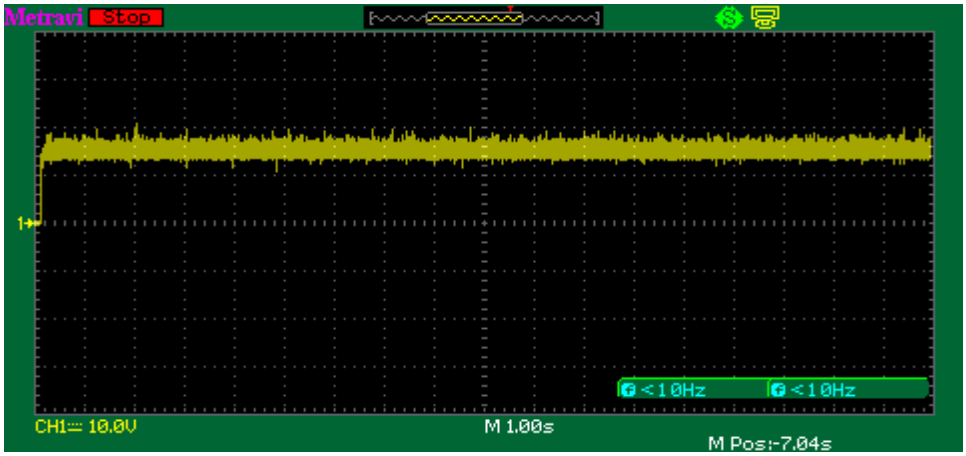
[Fig. 6] illustrates the operation of the newly introduced BLDC motor drive illustrating supply voltage, supply current, converter output voltage (Vout_l), motor speed, thenthe stator current and stator voltage for thedc link voltages of 16 V. A sinusoidalsupply current approximately in phase with the supply voltage is accomplished for operating at minimum dc link voltagethatindicates a near unitypower factor at the ac mains.



(a)Supply voltage

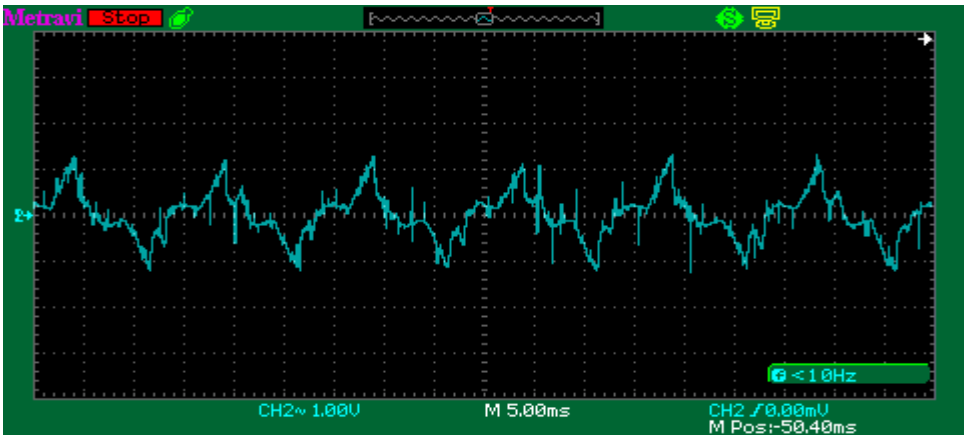


(b) Supply current

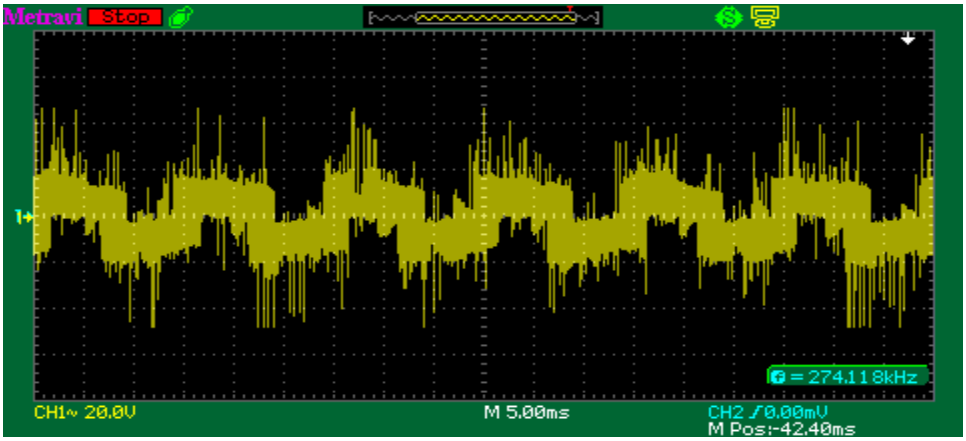


(C)BL TI-SEPIC converter output voltage ($Vout\_l$)

(d)BLDC motor speed in Rpm



(e) BLDC motor Stator current



(f) BLDC motor stator voltage

Fig.6: Test results of proposed BLDC motor driver for the dc link voltage of 16 V

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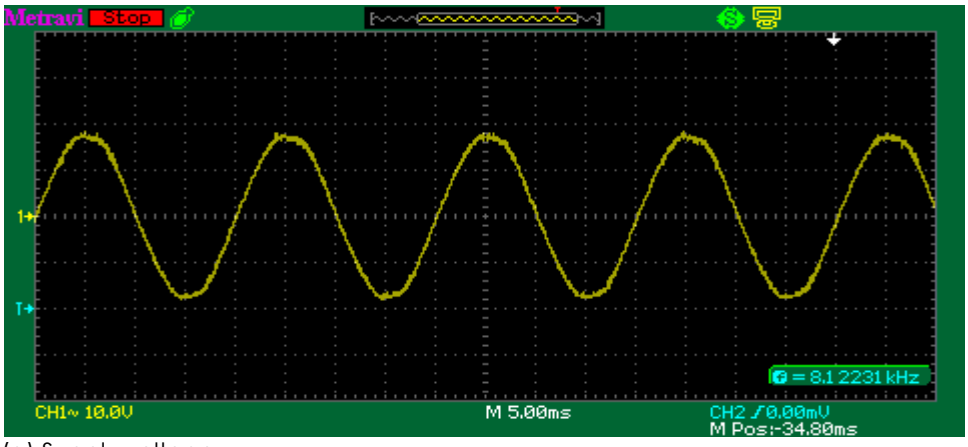
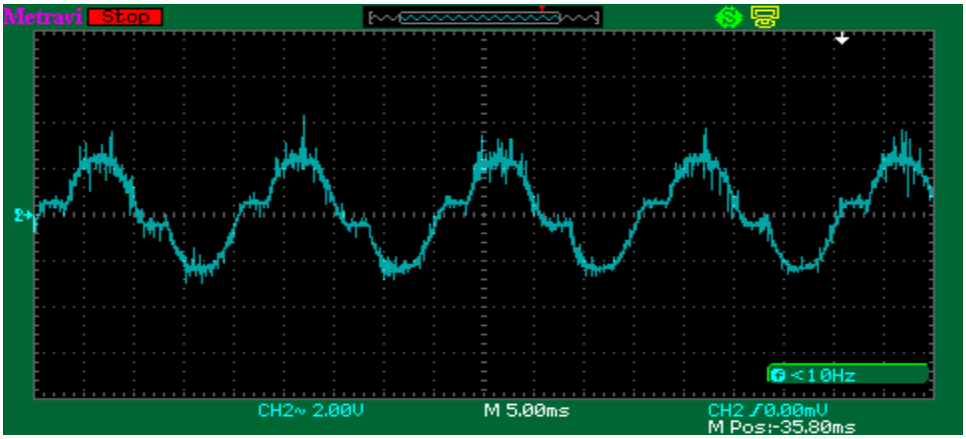
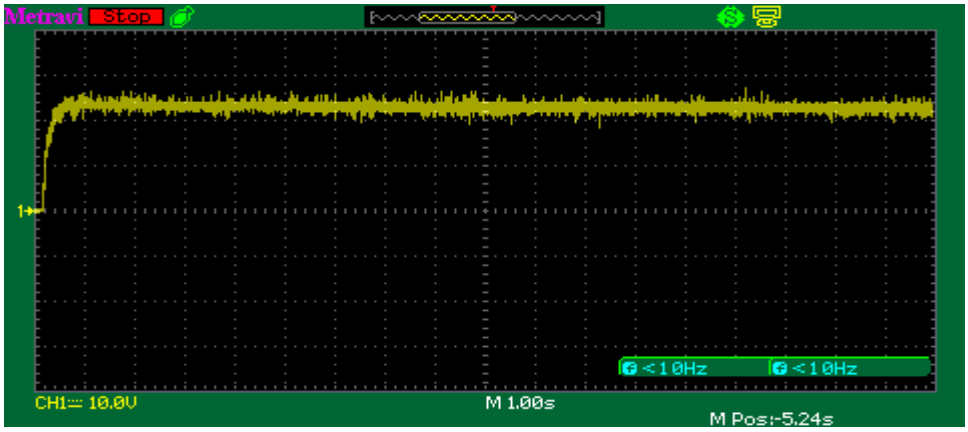
[Fig. 7] illustrates the operation of the newly introduced BLDC motor drive showing supply voltage, supply current, converter output voltage (Vout_m), motor speed, thereafter the stator current and stator voltage for thedc link voltages of 24V, correspondingly. A sinusoidalsupply current approximately in phase with the supply voltage is attained for operating at minimum dc link voltagethatindicates a near unitypower factor at ac mains.



(a) Supply voltage

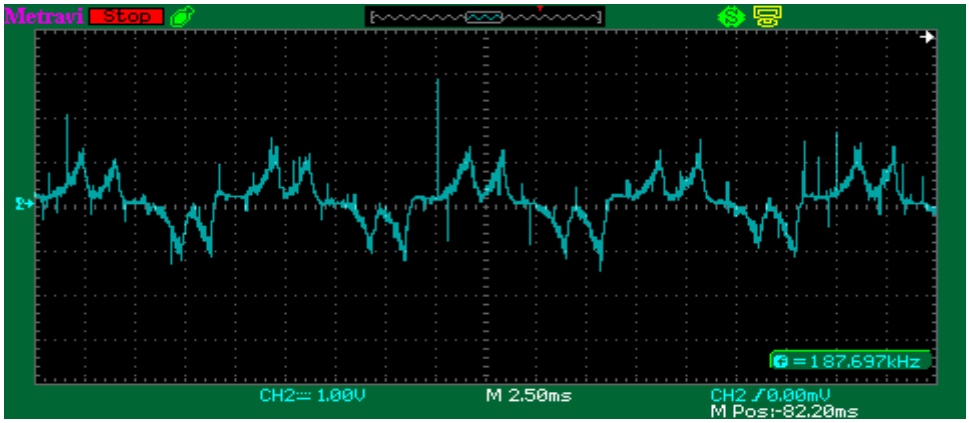


(b) Supply current

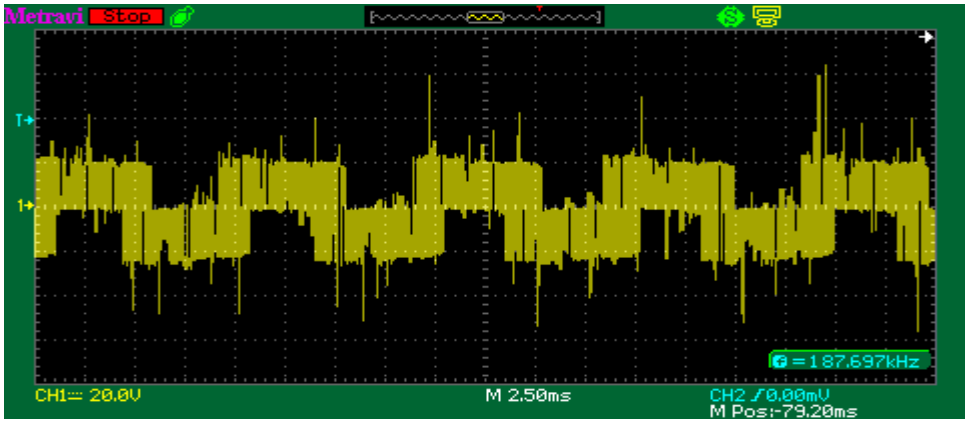


(c) BL TI-SEPIC converter output voltage

(d) BLDC motor speed in Rpm



(e) BLDC motor stator current



(f) BLDC motor stator voltage

Fig.7: Test results of proposed BLDC motor driver for the dc link voltage of 24 V

CONCLUSION

A PFC BL TI-SEPIC converter-based VSI-fed BLDC motor drive has been introduced aiming at low-power applications. A noveltechnique of speed control has been used by regulating the voltage at dc bus and then operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor in order to reduce the switching losses in VSI. The operation of the front-end BL TI-SEPIC converter has been done in DCM for attaining an intrinsic power factor correction at ac mains. A satisfying closed-loop performance has been accomplished for different speed control with enhanced power factor. At last, an experimental model of the driveproposed has been designed in order to verify the performance of the new BLDC motor drive under speed control with enhanced power quality at ac mains. The scheme proposed has revealeddesired performance, and it is a solutionrecommended to be appliedforhigh-power BLDC motor drives.

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