ISSN: 0976-3104
ISSUE: Computer and Allied Sciences

ARTICLE

A NOVEL DESIGN OF 1-BIT COMPARATOR USING QUANTUM-DOT CELLULAR AUTOMATA

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ABSTRACT

Background: *Quantum-dot Cellular Automata (QCA) is a transistor-less computation approach introduced as a renewal key to the fundamental limits faced by CMOS technology ensuring small size, high speed operation, high integration density, capacity and ultra-low power consumption. Quantum Dot cell is an artificial nano-scale molecule which does not require current flow to pass the information. Any digital circuit can be fully realized using QCA cells. The comparator is a vital digital circuit required to perform number of arithmetic operations in applications, like a PC.* ***Methods:*** *Comparison of the proposed approach with the previous approaches is realized, evaluated and verified by utilizing QCA Designer tool, a simulation tool for QCA circuits, Version 2.0.3.* ***Results:*** *In this paper, a novel design of a comparator in Quantum Dot Cellular Automata (QCA) technique has been proposed which is a promising design significantly declined in terms of effective area, latency and cell complexity, compared to other layouts, and its clock cycle is confined to bare minimum.* ***Conclusions:*** *Simulation of the proposed 1-bit comparator shows the advantage of the proposed approach over the previous approaches as it possesses approximately 73% reduction in total area and 74% reduction in total number of cell counts.*

KEY WORDS
QCADesigner tool version 2.0.3, Quantum-dot Cellular Automata, comparator; Quantum-dot Cell

Received: 24 Jan 2020
Accepted: 2 Mar 2020
Published: 10 Mar 2020

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INTRODUCTION

In 1965, the Gordon Moore law predicted that the capacity of computer chips would be doubled in approximately every 18 months. Till now, it has governed the development and performance of microprocessors very well [1]. The scaling of CMOS Technology has almost reached its physical limit, which has led to an extensive research for developing future generation ICs and discovery of new technologies. Quantum dot Cellular Automata is one of the emerging technologies at nano-scale level that has overcome the barrier of scaling. Lent et al proposed a physical implementation of an automaton using quantum-dot cells in 1993 [1]. It was first fabricated in the year 1997 [2]. Among other nano-scale level techniques, QCA has proved to be a better alternative because of its attractive features such as high-speed operation, low power consumption and small dimension. QCA does not use transistors [2]. Basically, QCA are array or wire of cells, which store information using electrons [3]. A digital comparator takes two numbers as inputs in binary form and determines whether one number is greater than, less than or equal to the other number [4]. Comparators are extensively used in central processing units and microcontrollers and thus have been researched upon and optimized in CMOS technology [4]. This paper deals with QCA based comparator designs as we have compared our proposed design with previous layouts.

A 1-bit magnitude comparator design consisting of 73 cells and 0.06μm2 area was proposed in [4]. Another design of a reversible 1-bit comparator without wire crossing was proposed in [5]. It is constructed by using the Single Feynman and TR circuit and consists of 117 cells and 0.182μm2 area. In the paper [6], a 1-bit comparator using the most recent EX-OR entryway has been introduced. The QCA implementation of the proposed design utilizes 180° clock phase shift wire crossing and consists of 60 cells. An optimized 1-bit comparator design having 50% enhancement in the cell count and 59% enhancement in occupied area is presented in [7]. An efficient layout entailing the lowest cell count, area and clock cycle compared to the previous works is introduced in [8].

MATERIALS AND METHODS

QCA BASICS

QCA cell

A QCA cell is made up of four quantum dots with two electrons occupying opposite location in two different quantum dots. The electrons occupy opposite or diagonal corners as they are governed by the principle of Coulomb's repulsive force. [Fig. 1(a)] shows QCA cell in which binary 1 and binary 0 are indicated by polarity +1 and -1 respectively.

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ISSN: 0976-3104

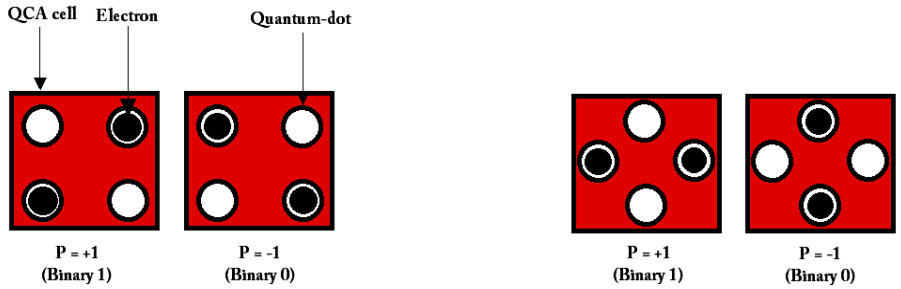

Fig. 1(a): QCA Cells

QCA Logic gate

The QCA Inverter and QCA Majority gate are the fundamental elements of any QCA circuit. A QCA Inverter is made up of minimum 2 QCA Cells in which one is an input cell and the other is output cell. On the other hand, a QCA Majority gate is made up of five QCA cells consisting of three input cells, a decision cell and an output cell. As a result of Coulomb's repulsive force in this structure, stable state of the output is dependant on the input. Hence electrons are placed at maximum distance.

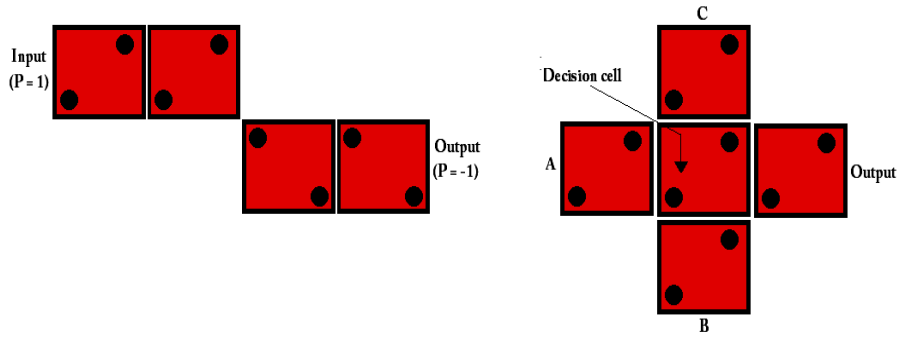

Fig. 1(b): QCA Inverter and Majority gate

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Wire crossing

The simplest arrangement of cells is given by placing quantum-dot cells in series. [Fig. 1(c)] shows such arrangement of four quantum-dot cells. The bounding boxes in the figure do not represent physical implementation, but it is shown to identify individual cells. If polarization of any cells in the arrangement shown in [Fig. 1(c-a)] is changed then rest of the cells are immediately synchronized to the new polarization due to coulombic interactions between them. There are two types of wires possible in QCA. A simple binary wire shown in [Fig. 1(c-a)] and an inverter chain, which has 45-degree inverted QCA cells side by side shown in [Fig. 1(c-b)].

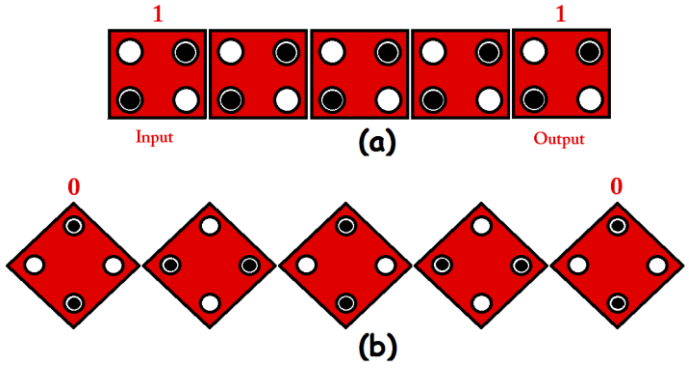

Fig. 1(c): (a) Series arrangement of QCA cells. **(b)** Series arrangement of 45-degree inverted QCA cells.

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ISSN: 0976-3104

QCA clocking

QCA clocking is used to determine data flow direction and also provides power to the circuit. It has four zones depending on the phases. There is a phase shift of 90°in each clocking zone. As shown in [Fig. 1(d)] there is four phases namely switch, hold, release and relax. In switch phase, electrons present in the quantum dots contain minimum energy after which the clock signal amplitude increases, potential energy of electrons begin to rise and finally the electrons gain the highest potential energy leading to the end of this phase. In the hold phase, also known as the high phase, electrons become effectively energized to exceed the tunneling barrier and the cells obtain null phase. In other words, the barriers are held at high value and the cell is now acting as an input to the next stage [9] .In the release phase, the high to low phase, actual computation is performed and electrons start to dissipate potential energy. [10] In the relax phase, the low phase, electrons bear minimum energy and are confined into the quantum dots. [10]

In QCA cells, having different colours means that they are under different clocks and having same colour means that they are under same clock. In QCA, Green refers to clock 0, Violet refers to clock 1, Blue refers to clock 2 and White refers to clock 3. [11]

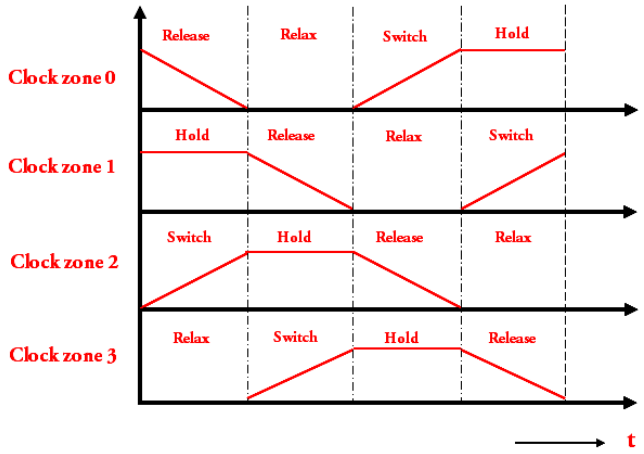

Fig. 1(d): Clocking in QCA

RESULTS

The proposed comparator design using QCA technology has two 1-bit inputs and three 1-bit outputs.

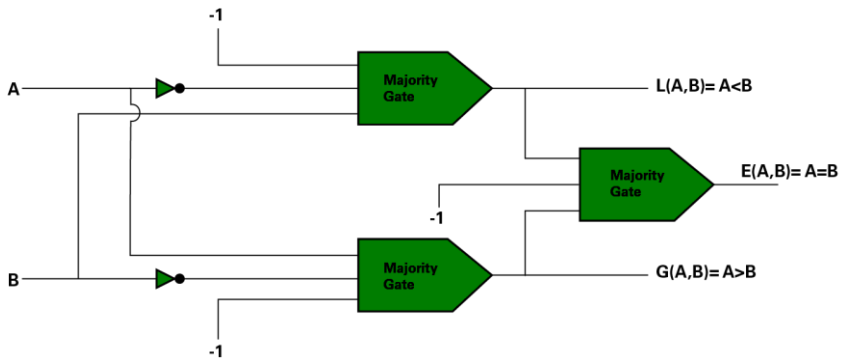

Fig. 2(a): Proposed 1-bit QCA comparator circuit

The inputs are indicated by A and B, and the outputs are indicated by L (A, B), E (A, B), and G (A, B). The relation between outputs and inputs are defined as follows.

L (A, B) =$\bar{A}$. B where A<B
E (A, B) = A$\bar{\odot}$B where A=B
G (A, B) = A. $\bar{B}$ where A>B

From the above equations it is observed that when input A is less than the input B, the output L (A, B) is "1" and it is "0" for E (A, B) and G (A, B). But if input A is greater than the input B, the output G (A, B) is "1" and other outputs remain "0". When both the inputs A and B are equal, only the output E (A, B) is "1". [8]

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ISSN: 0976-3104

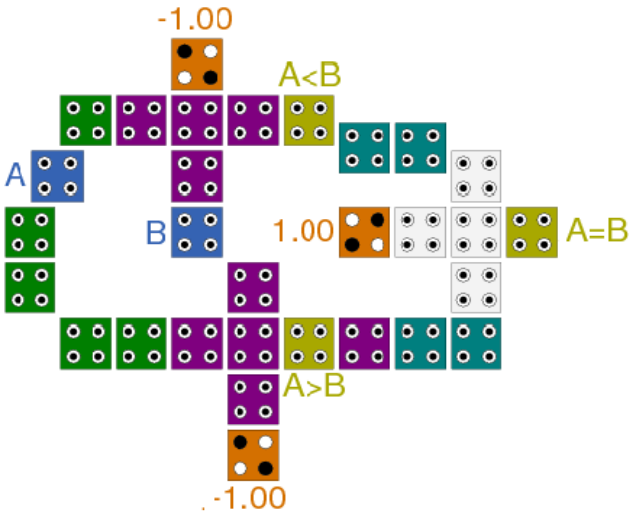

Fig. 2(b): Proposed 1-bit QCA comparator circuit

The layout design of proposed 1-bit comparator as shown in [Fig. 2(b)] consists of two inverters and three majority gates. The majority gates are used here for implementation of AND gates [8]. This layout of 1-bit QCA comparator circuit requires 30 number of QCA cells.

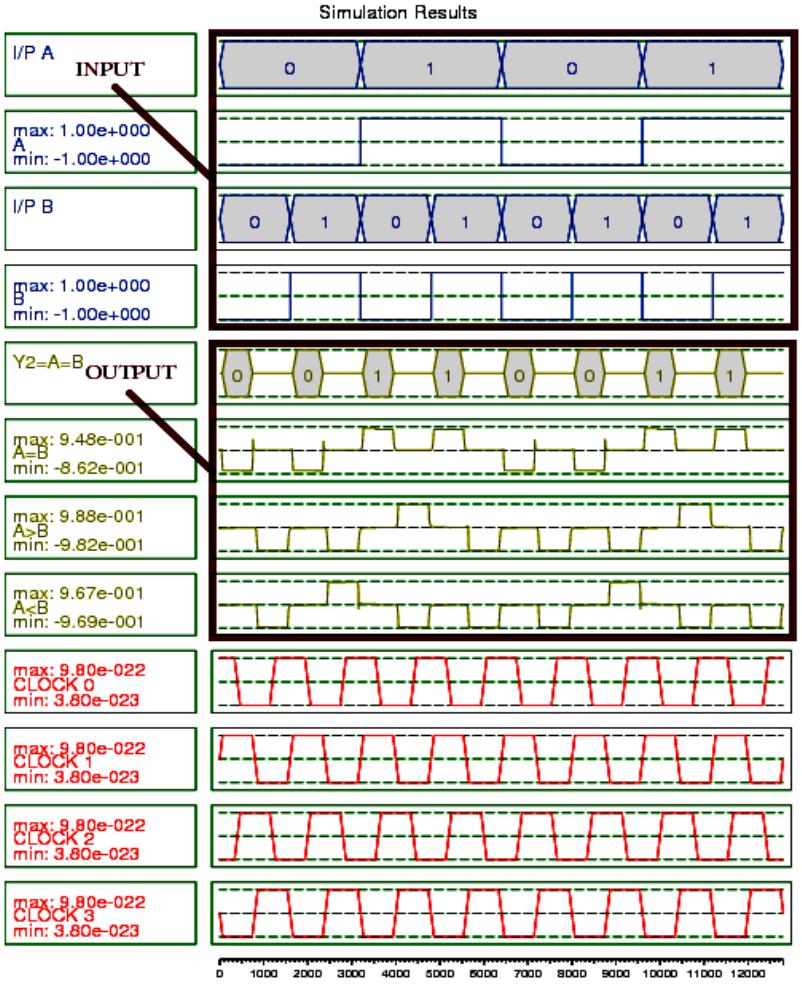

Fig. 2(c): Simulation for proposed QCA comparator

The outputs of the proposed 1-bit comparator circuit are correctly obtained after 1 clock cycle delay. It requires 0.05 μm2 area and 30 QCA cells.

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DISCUSSION

Table 1 shows the comparison of 1-bit Comparator with other comparators.

Various QCA comparator circuits mentioned in [Table 1] have shown good performance but improvements have been entailed in the proposed comparator.

Table 1: Comparison table for 1-bit comparators

Sr no.	Reported designs	Number of QCA Cells	Area (μm^2)	Time Delay (Clock Cycle)	Cost (Area× Clock cycles)
1	[1]	73	0.06	1	0.06
2	[4]	117	0.182	1	0.182
3	[3]	60	0.10	0.5	0.05
4	Proposed design	30	0.05	1	0.05

Area and delay are shown in terms μm2 and clock cycle respectively. To determine the cost, following equation can used [8]

Cost=Area × Delay

The proposed design of 1-bit Comparator has major advantages in terms of cost and area as compared to other designs [8].

Following is the graph denoting cell count, area occupied and cost of various comparators in comparison with the proposed layout.

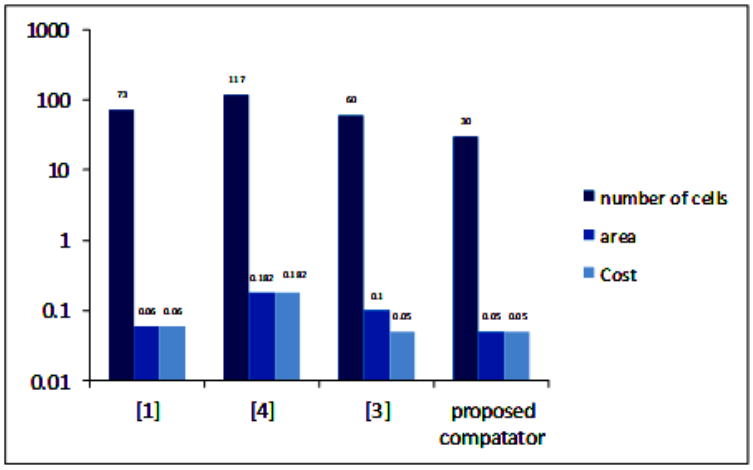

Fig. 3: Comparative analysis for number of cells, area and cost

The proposed comparator is seen to have lesser cell complexity, lesser area and lower cost compared to the previous designs.

CONCLUSION

In this paper, a new design of 1-bit comparator has been proposed, which is robust and efficient than the previous designs. It surpasses its counterparts in terms of area as well as complexity. The 1-bit QCA comparator circuit is carefully constructed using Majority gates, XNOR gates and Inverter gate. The functionality and efficiency of the proposed designs has been verified using QCA Designer 2.0.3 simulation tool. The obtained results indicate that the designed 1-bit comparator circuit requires 0.05 μm2 area, which is 73% less in total area compared to the previous designs and 74% less cell count compared to the previous designs, as only 30 QCA cells have been utilized. It has 1 clock cycle delay. In future, this design can be implemented in several calculative applications, which may perform a vital function of a general-purpose nano-processor as well as image processing applications.

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ISSN: 0976-3104

CONFLICT OF INTEREST

There is no conflict of interest.

ACKNOWLEDGEMENTS

We would like to express our sincere gratitude to our Principal Dr. Sanjay Pawar and our Head of Department Dr. Shikha Nema for their kind co-operation and encouragement which helped us in the completion of this project in timely manner.

FINANCIAL DISCLOSURE

No finance was provided for this study

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